Mobile DDR SDRAM

MT46H64M16LF – 16 Meg x 16 x 4 banks
MT46H32M32LF – 8 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

Features
- Endur-IC™ technology
- V_{DD}/V_{DDQ} = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data–one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive (DS)
- Clock stop capability
- 64ms refresh

Table 1: Configuration Addressing

Architecture	64 Meg x 16	32 Meg x 32
Configuration	16 Meg x 16 x 4 banks	8 Meg x 32 x 4 banks
Refresh count	8K	8K
Row addressing	16K (A0–A13)	8K (A0–A12)
Column addressing	1K (A0–A9)	1K (A0–A9)

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz) CL = 3	Access Time
-6	166	5.5ns
-75	133	6.0ns

Options   Marking
- V_{DD}/V_{DDQ}
  - 1.8V/1.8V   H
- Configuration
  - 64 Meg x 16 (16 Meg x 16 x 4 banks)   64M16
  - 32 Meg x 32 (8 Meg x 32 x 4 banks)   32M32
- Plastic package
  - 60-ball VFBGA (10mm x 11.5mm)[1]   CK
  - 90-ball VFBGA (10mm x 13mm)[2]   CM
- Timing – cycle time
  - 6ns @ CL = 3   -6
  - 7.5ns @ CL = 3   -75
- Operating temperature range
  - Commercial (0° to +70°C)   None
  - Industrial (–40°C to +85°C)   IT

Notes: 1. Only available for x16 configuration.
           2. Only available for x32 configuration.

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Figure 1:   1Gb Mobile DDR Part Numbering

Example Part Number: MT46H32M32LFXX-75IT

MT46	V$_{DD}$/V$_{DDQ}$	Mobile Configuration	Package	Speed	Temp.

V$_{DD}$/V$_{DDQ}$	
1.7V/1.95V	H

Operating Temp.	
	Standard
IT	Industrial Temp.

Configuration	
64 Meg x 16	64M16LF
32 Meg x 32	32M32LF

	Package
CK	10 x 11.5 VFBGA (lead-free)
CM	10 x 13 VFBGA (lead-free)

	Speed Grade
-6	$^tCK = 6.0ns$
-75	$^tCK = 7.5ns$

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA Part Marking Decoder is available at www.micron.com/decoder.

General Description

The 1Gb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 268,435,456-bit banks is organized as 16,384 rows by 1,024 columns by 16 bits. Each of the x32's 268,435,456-bit banks is organized as 8,192 rows by 1,024 columns by 32 bits.

The 1Gb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$-prefetch architecture with an interface designed to transfer four data words per clock cycle (x32), or two words per clock cycle (x16)at the I/O balls. A single read or write access for the 1Gb Mobile DDR SDRAM effectively consists of a single $2n$-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte and the x32 offering has four data strobes, one per byte.

The 1Gb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto-precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of Mobile DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained once the device enters deep power-down mode.

Micron's 1Gb Mobile DDR SDRAM device features Endur-IC technology. Pairing Micron's advanced memory architecture with innovative Endur-IC technology results in Mobile DDR devices that exceed current JEDEC standards, including lower power specifications that dramatically reduce overall power consumption.

Two self refresh features, temperature-compensated self refresh (TCSR) and partial-array self refresh (PASR), offer additional power savings. TCSR is controlled by the automatic on-chip temperature sensor. The PASR can be customized using the extended mode register settings. The two features may be combined to achieve even greater power savings.

Notes: 1. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.

2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

Figure 2:   Functional Block Diagram (64 Meg x 16)
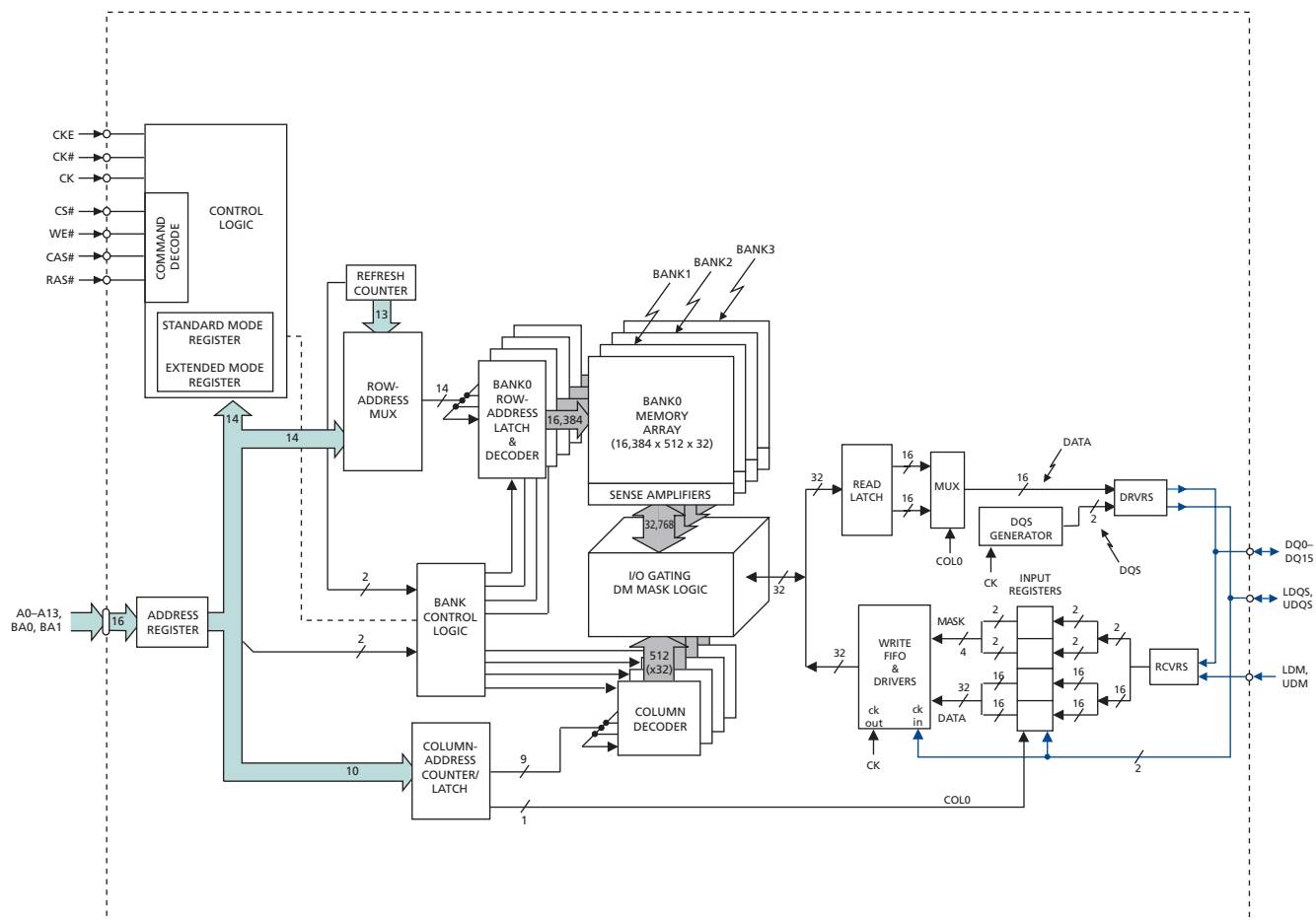
Figure 3:   Functional Block Diagram (32 Meg x 32)
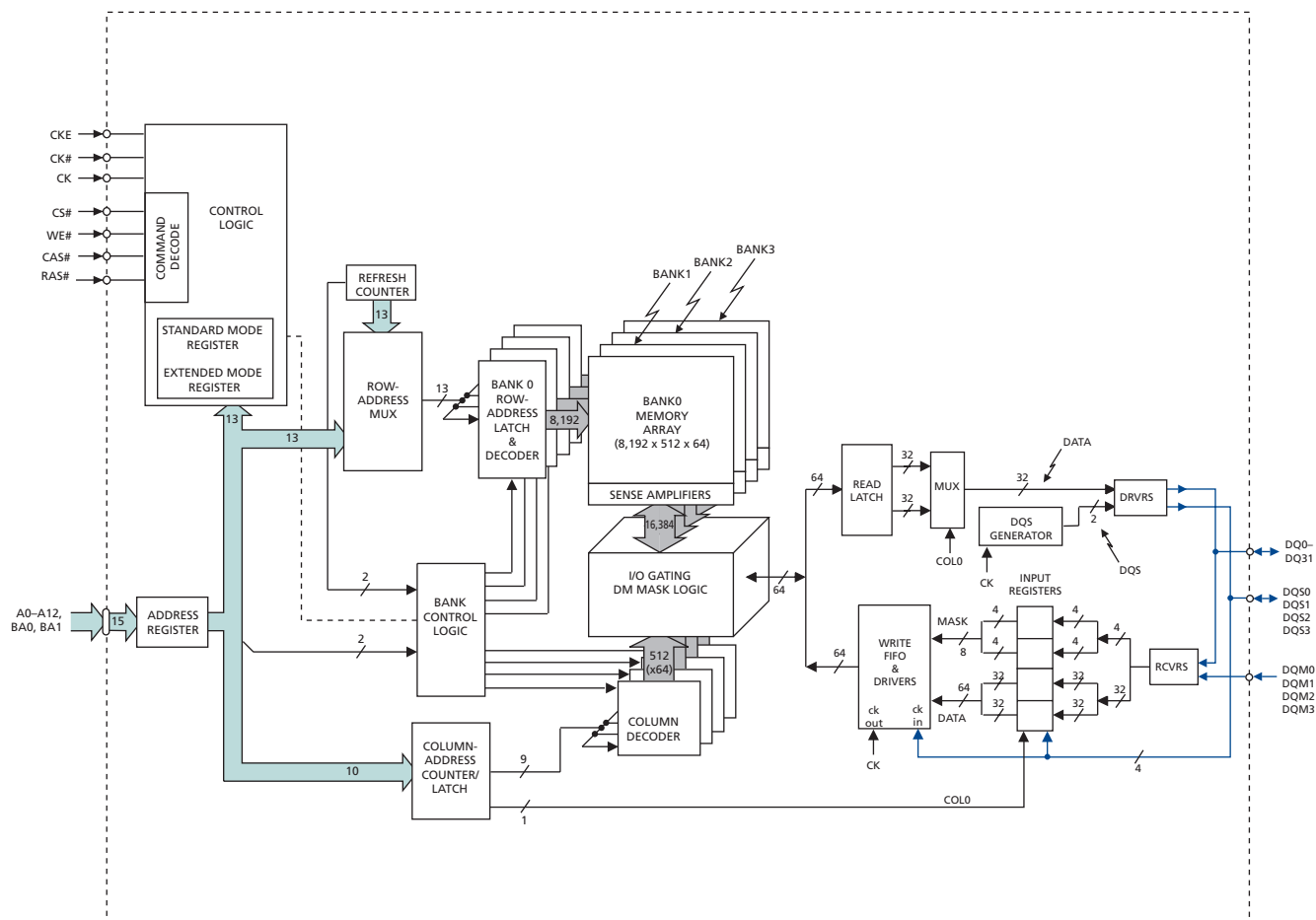
Ball Assignments and Descriptions

Figure 4:   60-Ball VFBGA Assignment – 10mm x 11.5mm (Top View)

	1	2	3	4	5	6	7	8	9
A	Vss	DQ15	VssQ				VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14				DQ1	DQ2	VssQ
C	VssQ	DQ11	DQ12				DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10				DQ5	DQ6	TEST[1]
E	VssQ	UDQS	DQ8				DQ7	LDQS	VDDQ
F	Vss	UDM	NC				A13	LDM	VDD
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	Vss	A4	A5				A2	A3	VDD

Ball and Array

Notes: 1. D9 is a test pin that must be tied to Vss or VssQ in normal operations.

Figure 5:   90-Ball VFBGA Ball Assignment – 10mm x 13mm (Top View)

	1	2	3	4	5	6	7	8	9
A	Vss	DQ31	VssQ				VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30				DQ17	DQ18	VssQ
C	VssQ	DQ27	DQ28				DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26				DQ21	DQ22	TEST[1]
E	VssQ	DQS3	DQ24				DQ23	DQS2	VDDQ
F	VDD	DM3	NC				NC	DM2	Vss
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	VssQ	DQS1	DQ8				DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10				DQ5	DQ6	VssQ
N	VssQ	DQ11	DQ12				DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14				DQ1	DQ2	VssQ
R	Vss	DQ15	VssQ				VDDQ	DQ0	VDD

Ball and Array

Notes: 1. D9 is a test pin that must be tied to Vss or VssQ in normal operations.

Table 3: 60-Ball FBGA Ball Description

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F2, F8	UDM, LDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15.
H8, H9	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K8, K2, K3, J1, J2, J3, H1, J7, H2, H3, F7	A0–A13	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto-precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ15	I/O	Data input/output: Data bus for x16.
E8, E2	LDQS, UDQS	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.
A7, B1, C9, D1, E9	V$_{DD}$Q	Supply	DQ power supply
A3, B9, C1, E1	V$_{SS}$Q	Supply	DQ ground
A9, F9, K9	V$_{DD}$	Supply	Power supply
A1, F1, K1	V$_{SS}$	Supply	Ground
F3	NC	–	No connect: F3 may be left unconnected.
D9	TEST	–	D9 is a test pin that must be tied to V$_{SS}$ or V$_{SS}$Q in normal operations.

Table 4:   90-Ball VFBGA Ball Description

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
K8, K2, F8, F2	DM0–DM3	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x32, DM0 is DM for DQ0–DQ7; DM1 is DM for DQ8–DQ15; DM2 is DM for DQ16–DQ23; DM3 is DM for DQ24–DQ31.
H8, H9	BA0, BA1	Input	Bank address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K9, K1, K3, J1, J2, J3, H1, J7, H2, H3, F7	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto-precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
D9	TEST	–	D9 is a test pin that must be tied to Vss or VssQ in normal operations.
F3, F7	NC	–	No connect; may be left unconnected.
R8, P7, P8, N7, N8, M7, M8, L7 L3, M2, M3, N2, N3, P2, P3, R2, A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ31	I/O	Data input/output: Data bus for x32.
L8, L2, E8, E2	DQS0–DQS3	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data.
A7, B1, C9, D1, E9, L9, M1, N9, P1, R7	V_{DD}Q	Supply	DQ power supply

Table 4:   90-Ball VFBGA Ball Description (continued)

Ball Numbers	Symbol	Type	Description
A3, B9, C1, E1, L1, M9, N1, P9, R3	VssQ	Supply	DQ ground
A9, F1, R9	VDD	Supply	Power supply
A1, F9, R1	Vss	Supply	Ground

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Functional Description

The 1Gb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 268,535,456-bit banks is organized as 16,384 rows by 1,024 columns by 16 bits. Each of the x32's 268,535,456bit banks is organized as 8,192 rows by 1,024 columns by 32 bits.

The 1Gb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 1Gb Mobile DDR SDRAM consists of a single $2n$-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine must be followed to ensure proper functionality of the Mobile DDR SDRAM.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. The core power (VDD) and I/O power (VDDQ) must be brought up simultaneously. It is recommended that VDD and VDDQ be from the same power source or VDDQ must never exceed VDD. Assert and hold CKE HIGH.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs minimum delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least ^{t}RP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least ^{t}RFC time. Two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO REFRESH command and NOP or DESELECT sequence can be issued after step 10.

7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.

8. Issue NOP or DESELECT commands for at least ^{t}MRD time.

9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.

10. Issue NOP or DESELECT commands for at least ^{t}MRD time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device.

Standard Mode Register

The standard mode register bit definition allows the selection of burst length, burst type, CAS latency, and operating mode, as shown in Figure 6 on page 16. Reserved states should not be used as it may result in setting the device into an unknown state or cause incompatibility with future versions of Mobile DDR SDRAMs. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating any of these requirements will result in unspecified operation.

Figure 6:   Standard Mode Register Definition

M15	M16	Mode Register Definition
0	0	Standard mode register
0	1	Status register read
1	0	Extended mode register
1	1	Reserved

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M13	M12	M11	M10	M9	M8	M7	M6 M5 M4 M3 M2 M1 M0	Operating Mode
0	0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	–	–	All other states reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length (BL) being programmable (see Table 5 on page 18 for details). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both sequential and interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, and by A3–Ai when BL = 8, where Ai is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved via the standard mode register.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address. See Table 5 on page 18 for details.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first output data. The latency can be set to 2 or 3 clocks, as shown in Figure 7.

For CL = 3, if the READ command is registered at clock edge n, then the data will nominally be available at (n + 2 clocks + ^{t}AC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally be available at (n + 1 clock + ^{t}AC).

Figure 7:   CAS Latency
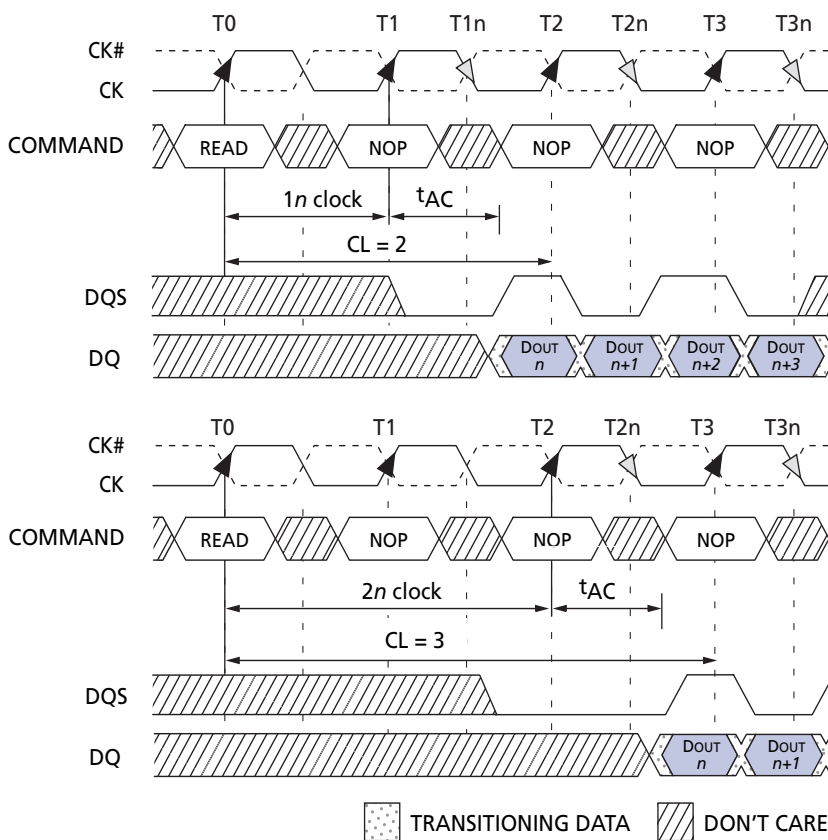
Table 5: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER command with bits A7–A12 (x32) or A7–A13 (x16) each set to zero, and bits A0–A6 set to the desired values.

All other combinations of values for A7–A12/A13 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls additional functions beyond those set by the mode registers. These additional functions include drive strength, temperature-compensated self refresh, and partial-array self refresh.

The extended mode register is programmed via the LOAD MODE REGISTER command with BA0 = 0 and BA1 = 1. Information in the extended mode register will be retained until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Temperature-Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator. Programming of the TCSR bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial-Array Self Refresh

For further power savings during self refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during self refresh. The refresh options are shown in

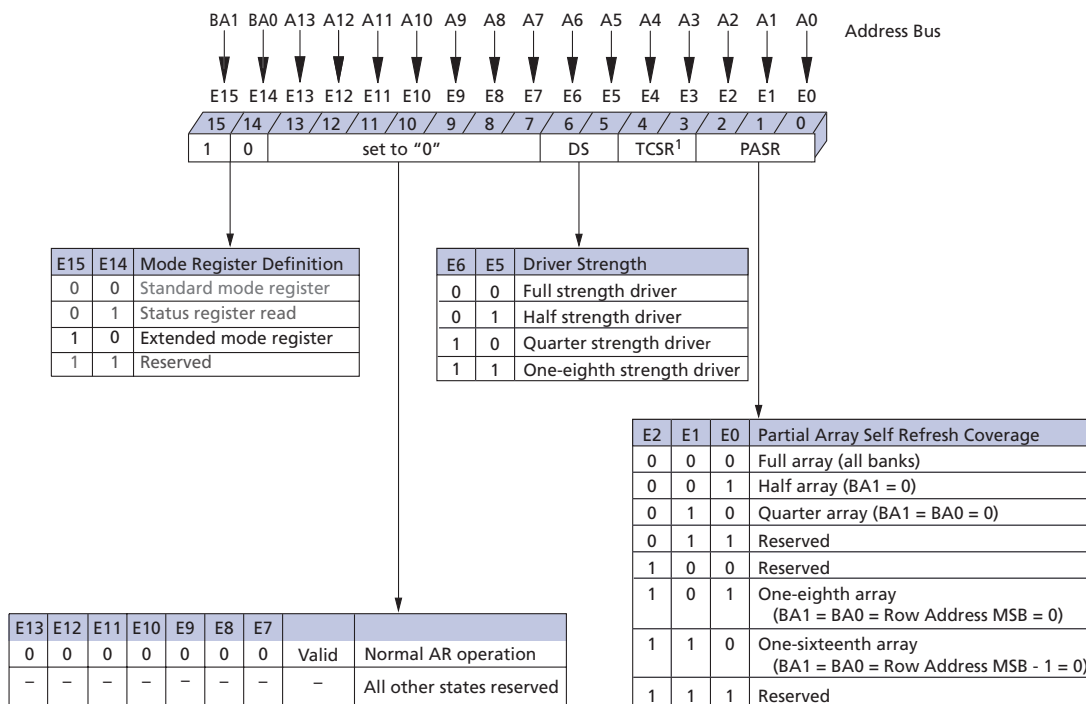WRITE and READ commands can still occur during standard operation, but only the selected regions of the array will be refreshed during self refresh. Data in regions that are not selected will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four allowable settings for the output drivers—25Ω, 55Ω, 80Ω, and 100Ω internal impedance. These are full, half, quarter, and one-eighth drive strengths, respectively. Target output drive characteristics can be found in Table 18 on page 64 and Table 19 on page 65 for full and half drive settings.

Figure 8:   Extended Mode Register

E15	E14	Mode Register Definition
0	0	Standard mode register
0	1	Status register read
1	0	Extended mode register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full strength driver
0	1	Half strength driver
1	0	Quarter strength driver
1	1	One-eighth strength driver

E2	E1	E0	Partial Array Self Refresh Coverage
0	0	0	Full array (all banks)
0	0	1	Half array (BA1 = 0)
0	1	0	Quarter array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array (BA1 = BA0 = Row Address MSB = 0)
1	1	0	One-sixteenth array (BA1 = BA0 = Row Address MSB - 1 = 0)
1	1	1	Reserved

E13	E12	E11	E10	E9	E8	E7		
0	0	0	0	0	0	0	Valid	Normal AR operation
–	–	–	–	–	–	–	–	All other states reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

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Status Register Read (SRR)

The status register read (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the Mobile SDRAM as shown in Figure 10. The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

1. The SDRAM must be properly initialized and in the idle or all banks precharged state.
2. Issue a LOAD MODE REGISTER command with BA[1:0] = "01."
3. Wait ^{t}SRR; NOP or DESELECT commands are only allowed during the ^{t}SRR time.
4. Issue a READ command with all address pins set to "0."
5. Subsequent commands to the SDRAM must be issued ^{t}SRC after the SRR READ command is issued; only NOPs or DESELCTS are allowed during ^{t}SRC (See Figure 10: "Status Register Definition" on page 21).

SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first bit of the burst, with the output being "don't care" on the second bit of the burst.

Figure 9:   SRR Timing
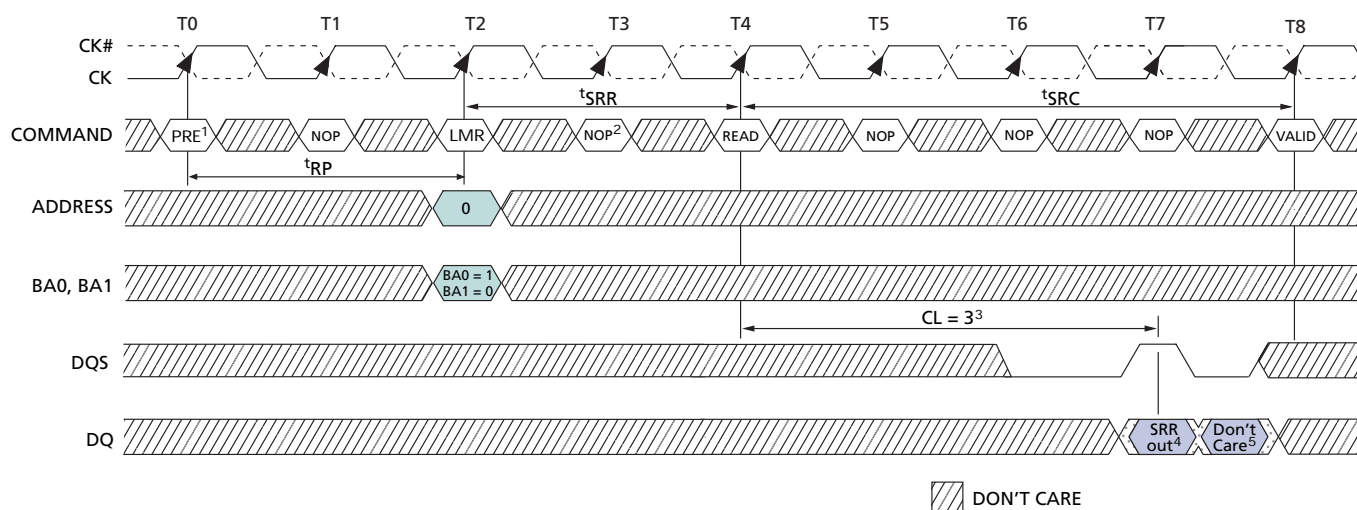
Notes: 1. All banks must be idle prior to status register read.
2. NOP or DESELECT commands are required between LMR and READ command (^{t}SRR), and between READ and next VALID command (^{t}SRC).
3. CAS latency is pre-determined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data out burst is a "don't care."

Figure 10: Status Register Definition
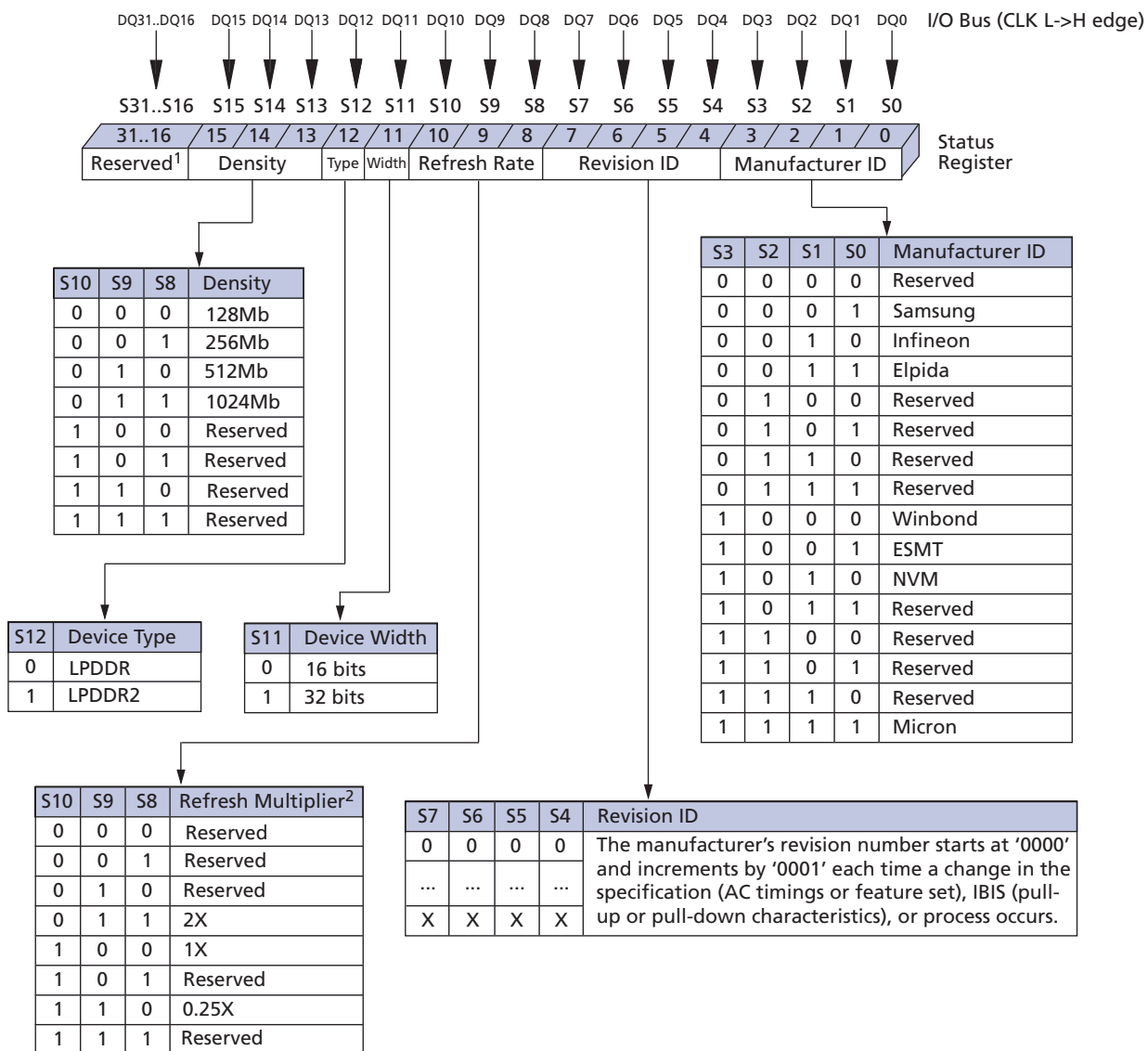
Notes: 1. Reserved bits should be set to zero (0) for future compatibility.
2. Refresh multiplier is based on the memory device's on-board temperature sensor. Required average periodic refresh interval = ^tREFI * multiplier.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock that controls the DDR SDRAM. There are two ways to control the clock:

1. Change the clock frequency.
2. Stop the clock.

The Mobile DDR SDRAM allows the clock to change frequency during operation only if all the timing parameters are met and all refresh requirements are satisfied.

The clock can be stopped altogether if there are no DRAM operations in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: ^{t}RCD, ^{t}RP, ^{t}RFC, ^{t}MRD, ^{t}WR, and all data-out for READ bursts.

For example, if a WRITE or a READ is in progress, the entire data burst must be complete prior to stopping the clock. For READs, a burst completion is defined when the read postamble is satisfied. For WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied.

CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued. Figure 11 on page 22 illustrates the clock stop mode.

Figure 11: Clock Stop Mode
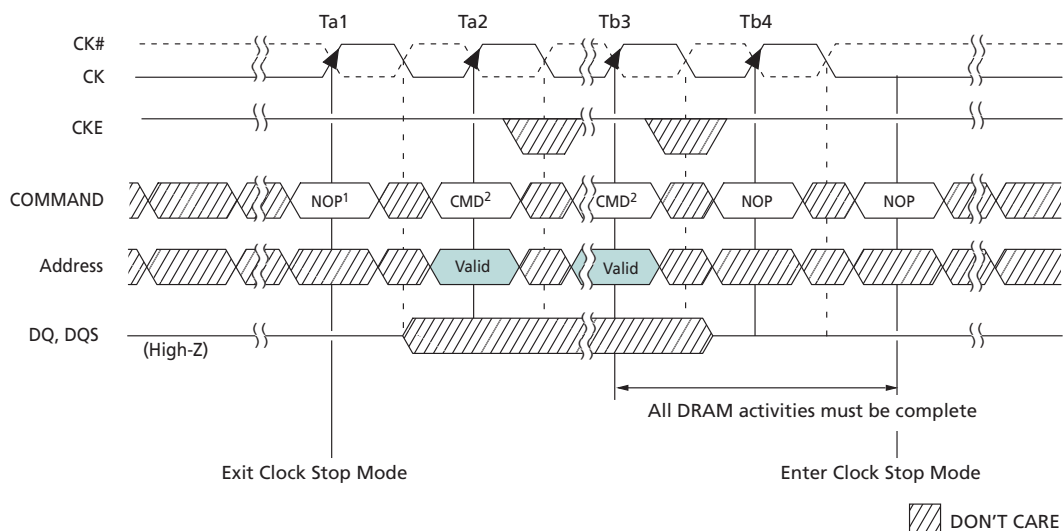
Notes: 1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
  2. Any valid command is allowed; device is not in clock suspend mode.

Commands

Table 6 and Table 7 provide a quick reference of available commands. This is followed by a written description of each command. Three additional truth tables (Table 8 on page 49, Table 9 on page 50, and Table 10 on page 52) provide CKE commands and current/next state information.

Table 6:   Truth Table – Commands
Notes 1 and 2 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT (NOP)	H	X	X	X	X	3
NO OPERATION (NOP)	L	H	H	H	X	3
ACTIVE (select bank and activate row)	L	L	H	H	Bank/row	4
READ (select bank and column, and start READ burst)	L	H	L	H	Bank/column	5
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	Bank/column	5
BURST TERMINATE or deep power-down (enter deep power-down mode)	L	H	H	L	X	6, 7
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	8
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	9, 10
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-code	11

Notes: 1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
2. All states and sequences not shown are reserved and/or illegal.
3. DESELECT and NOP are functionally interchangeable.
4. BA0–BA1 provide bank address and A0–A12/A13 provide row address.
5. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent); A10 LOW disables the auto precharge feature.
6. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
7. This command is a BURST TERMINATE if CKE is HIGH and deep power-down if CKE is LOW.
8. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
9. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
10. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
11. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12/A13 provide the op-code to be written to the selected mode register.

Table 7:   DM Operation Truth Table

Name (Function)	DM	DQ	Notes
Write enable	L	Valid	1, 2
Write inhibit	H	X	1, 2

Notes: 1. Used to mask write data; provided coincident with the corresponding data.
2. All states and sequences not shown are reserved and/or illegal.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. Operations already in progress are not affected.

Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained once the device enters deep power down mode.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected Mobile DDR SDRAM to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A12/A13. See mode register descriptions in "Register Definition" on page 15. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8/A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. The exception is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise, BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in "Operations" on page 27. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts with auto precharge disabled. The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown on page 33. The open page that the READ was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAMs. The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 1Gb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although it is not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to allow for future functional features. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except that CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH. See Figure 45 on page 72 for details on entering and exiting self refresh mode. During SELF REFRESH, the device is refreshed as identified in the extended mode register (see PASR setting).

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued for ^{t}XSR, in order to complete any internal refresh already in progress.

Figure 12:   Mobile DRAM State Diagram

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 13.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 13:   Activating a Specific Row in a Specific Bank
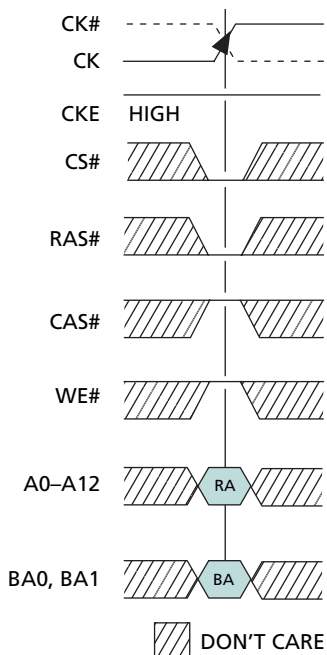
Notes: 1. BA = bank address.
RA = row address.

READs

READ burst operations are initiated with a READ command, as shown in Figure 14 on page 29.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (for example, at the next crossing of CK and CK#). Figure 15 on page 30 shows general timing for each possible CAS latency setting. DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 33 on page 46. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 40 on page 68.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$-prefetch architecture). This is shown in Figure 16 on page 31.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 17 on page 32. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 18 on page 32.
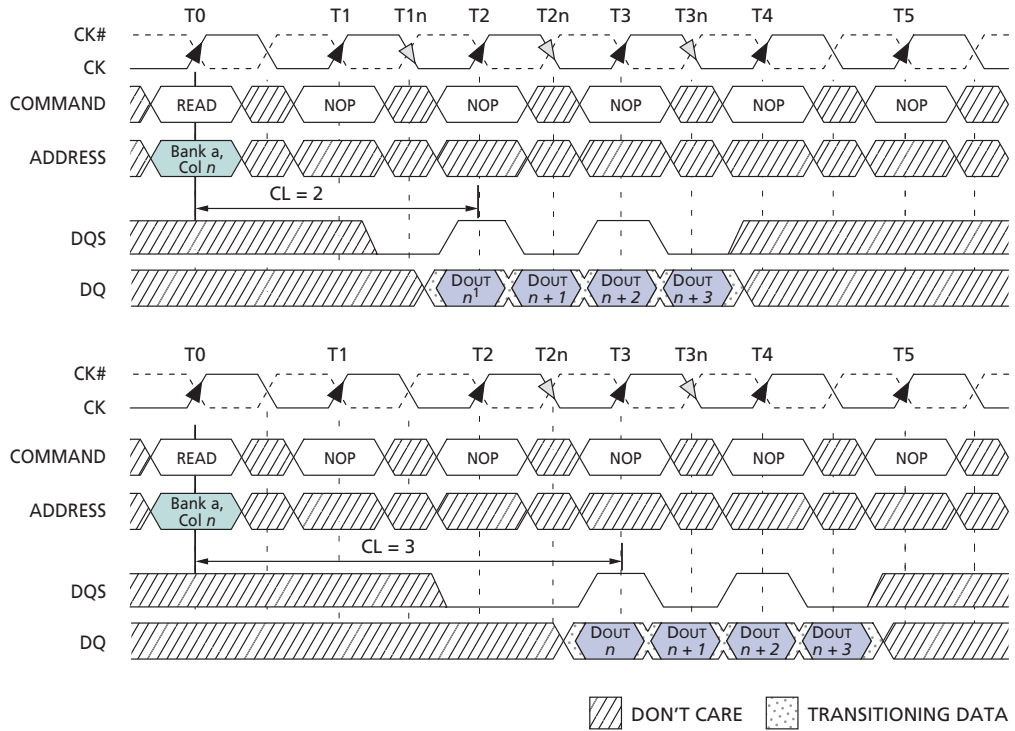
Figure 14: READ Command
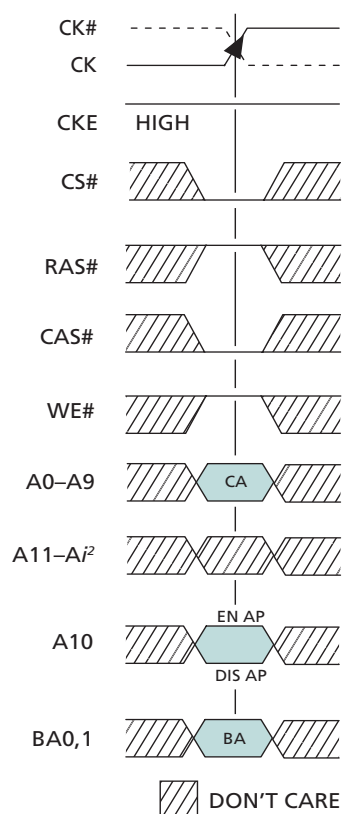
Notes: 1. CA = column address.
BA = bank address.
EN AP = enable auto precharge.
DIS AP = disable auto precharge.
2. i = the most significant column address bit for each configuration.

Figure 15:   READ Burst

Notes: 1. Dout *n* = data-out from column *n*.

Figure 16:   Consecutive READ Bursts
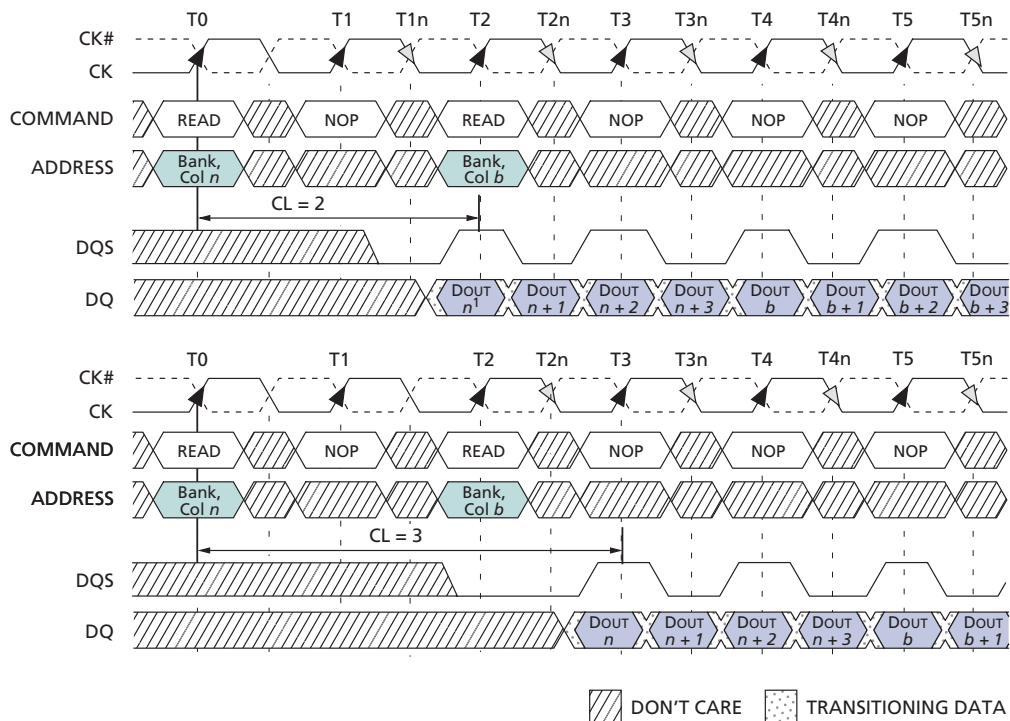
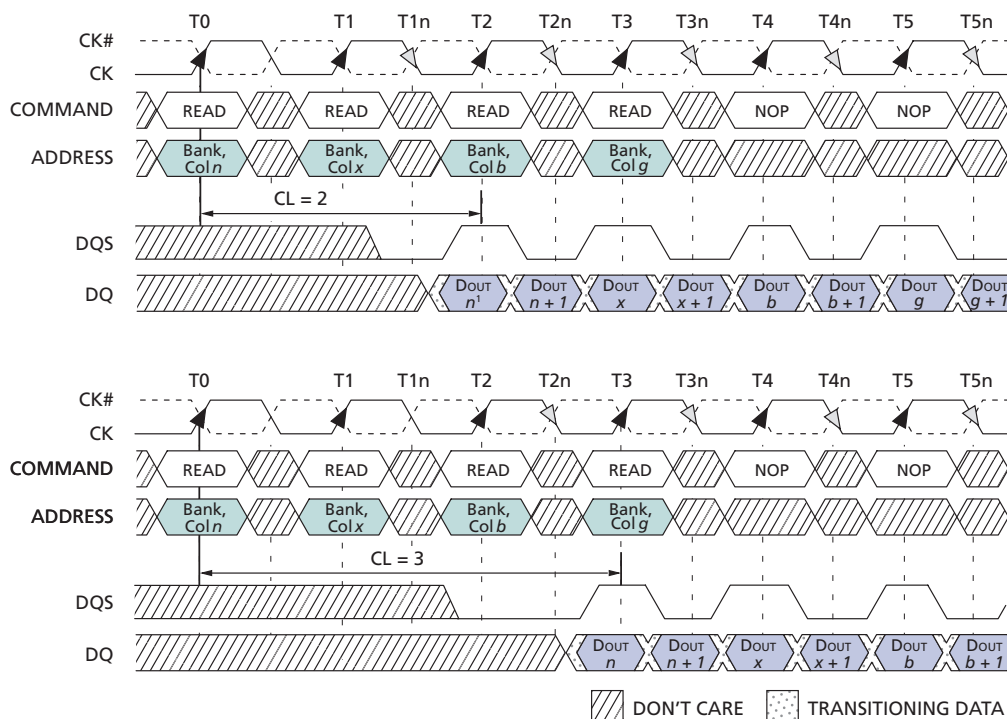Notes: 1. Dout *n* (or *b*) = data-out from column *n* (or column *b*).

Figure 17:   Nonconsecutive READ Bursts

DON'T CARE   TRANSITIONING DATA

Notes: 1. Dᴏᴜᴛ *n* (or *b*) = data-out from column *n* (or column *b*).

Figure 18:   Random READ Accesses

DON'T CARE   TRANSITIONING DATA

Notes: 1. Dᴏᴜᴛ *n* (or *x*, b, *g*) = data-out from column *n* (or column *x*, column *b*, column *g*).

Truncated READs

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 17. The BURST TERMINATE latency is equal to the READ (CAS) latency; for example, the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 18. The ^tDQSS (MIN) case is shown; the ^tDQSS (MAX) case has a longer bus idle time. (^tDQSS [MIN] and ^tDQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the n-prefetch architecture). This is shown in Figure 21 on page 35. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^tRP is met.

Note: Part of the row precharge time is hidden during the access of the last data elements.
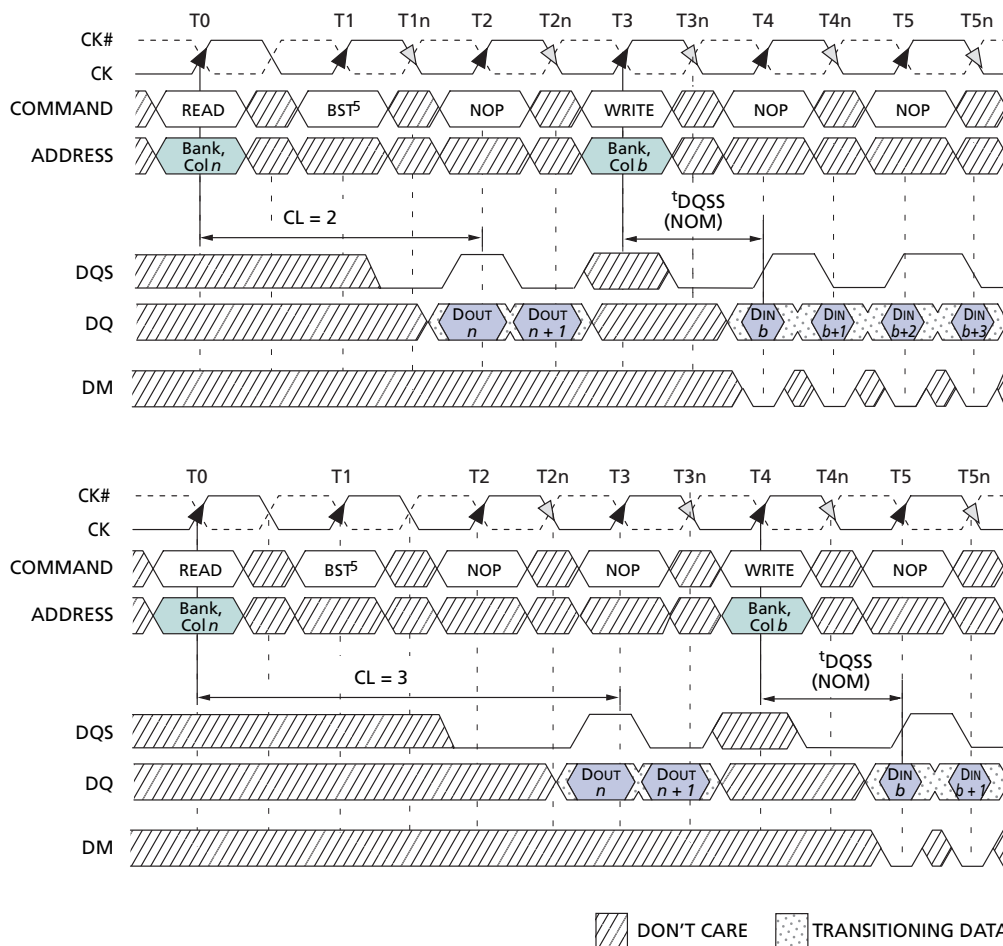
Figure 19:   Terminating a READ Burst
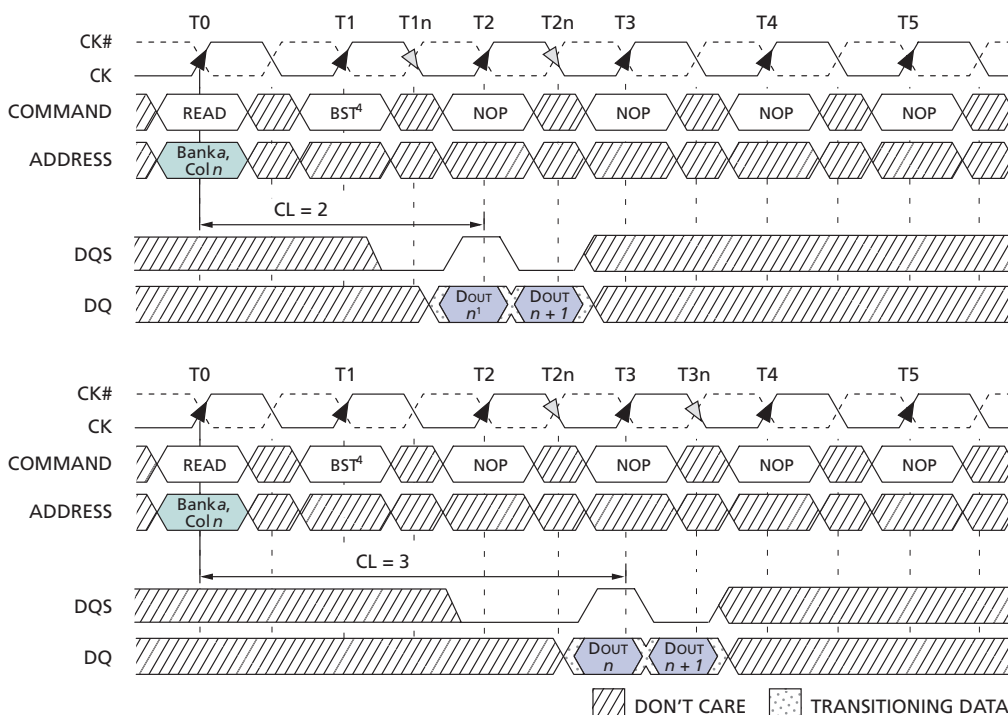
Notes: 1. Dout n = data-out from column n.

Figure 20: READ-to-WRITE
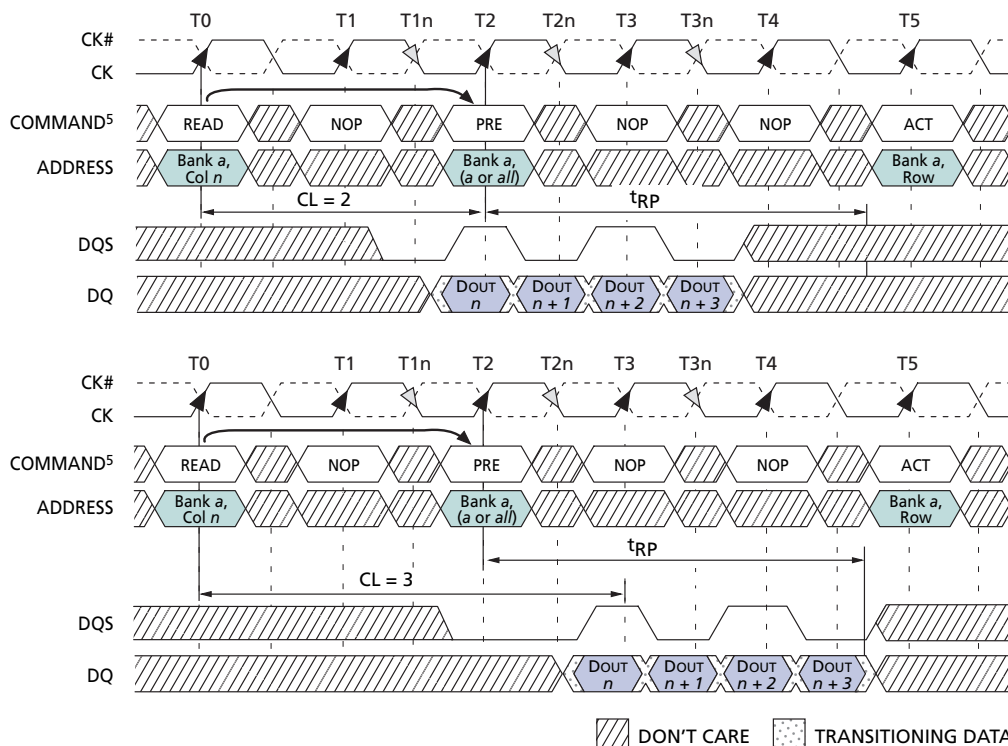

| | DON'T CARE | TRANSITIONING DATA |

Notes:
1. D_{OUT} n = data-out from column n.
2. D_{IN} b = data-in from column b.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.

Figure 21: READ-to-PRECHARGE

Notes:
1. D$_{OUT}$ n = data-out from column n.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided ^{t}RAS (MIN) is met, would cause a precharge to be performed at x number of clock cycles after the READ command, where x = BL/2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 22 on page 37.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (for example, ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 23 on page 38 shows the nominal case and the extremes of ^{t}DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the $2n$-prefetch architecture).

Figure 24 on page 38 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 25 on page 39. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 26 on page 39.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, ^{t}WTR should be met, as shown in Figure 27 on page 40.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 28 on page 41. Note that only the data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 29 on page 42.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, ^{t}WR should be met, as shown in Figure 30 on page 43.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 28 on page 41 and Figure 32 on page 45. Note that only the data-in pairs that are registered prior to the ^{t}WR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 28 on page 41 and Figure 32 on page 45. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.
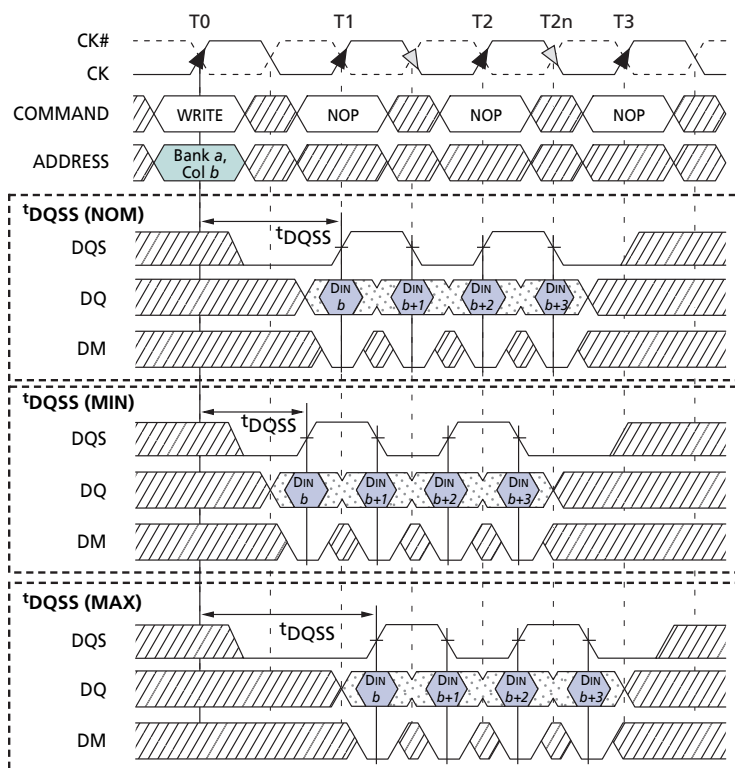
Figure 22:   WRITE Command
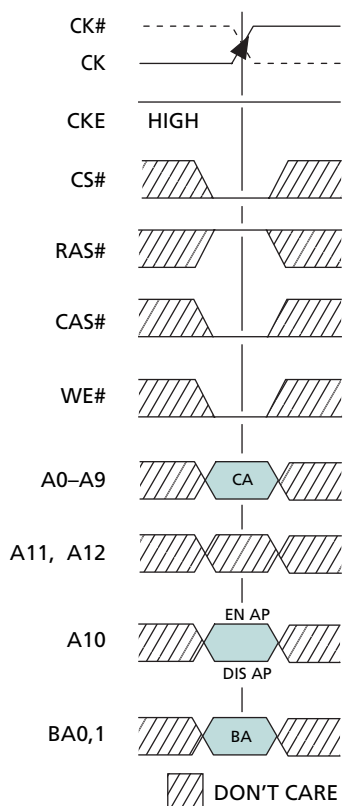
Notes: 1. CA = column address.
BA = bank address.
EN AP = enable auto precharge.
DIS AP = disable auto precharge.
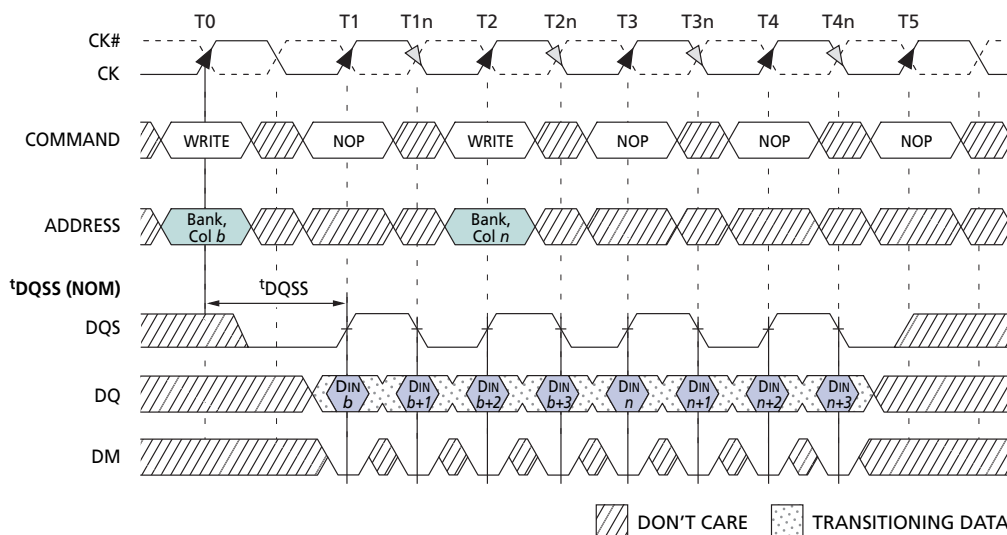
Figure 23:   WRITE Burst

Notes: 1.   DIN b = data-in for column b.
            2.   An uninterrupted burst of 4 is shown.
            3.   A10 is LOW with the WRITE command (auto precharge is disabled).
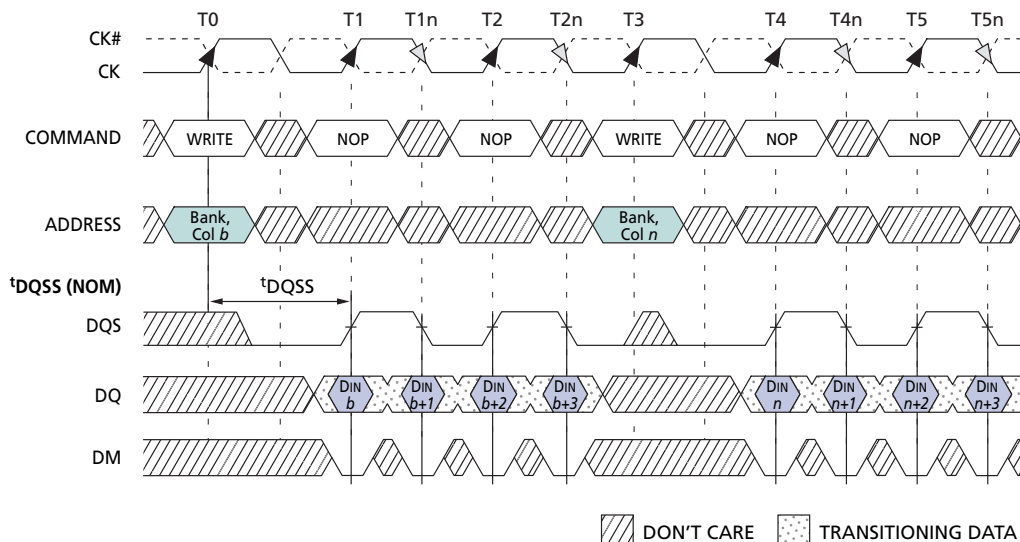
Figure 24:   Consecutive WRITE-to-WRITE

Notes: 1.   DIN b (n) = data-in for column b (n).
            2.   An uninterrupted burst of 4 is shown.
            3.   Each WRITE command may be to any bank.

Figure 25:   Nonconsecutive WRITE-to-WRITE

Notes: 1. DIN b (n) = data-in for column b (n).
         2. An uninterrupted burst of 4 is shown.
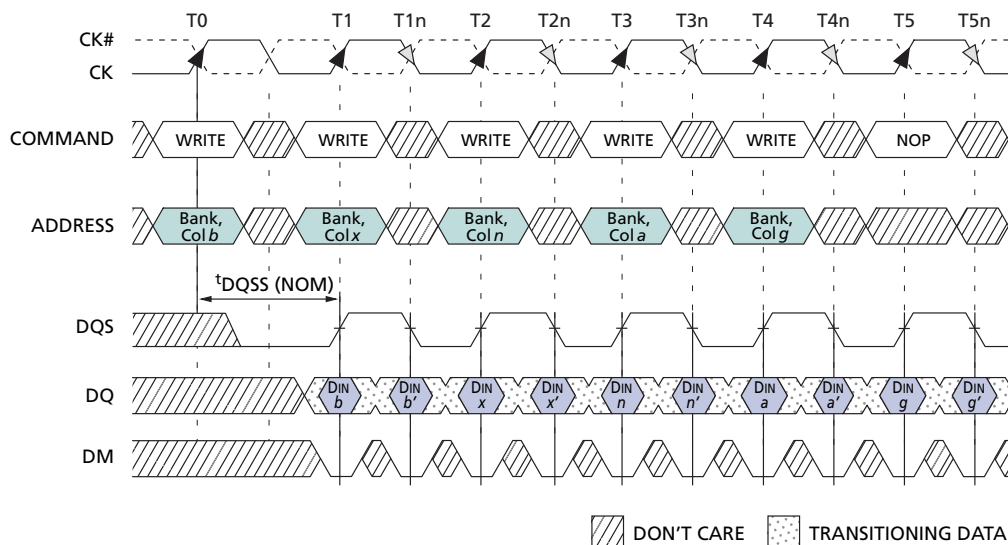   3. Each WRITE command may be to any bank.

Figure 26:   Random WRITE Cycles
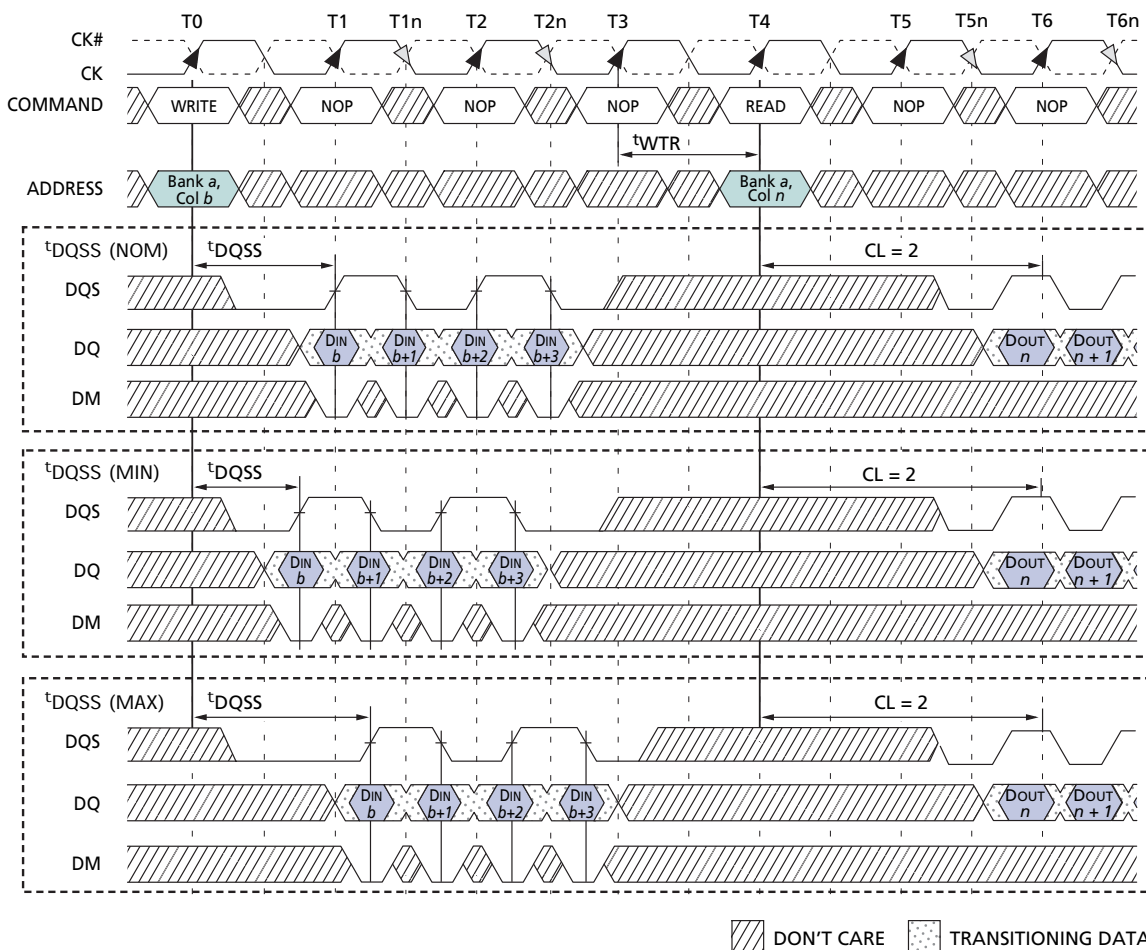

Notes: 1. DIN b (or x, n, a, g) = data-in for column b (or x, n, q, g).
         2. b' (or x, n, a, g) = the next data-in following DIN b (x, n, a, g) according to the programmed burst order.
         3. Programmed BL = 2, 4, or 8 in cases shown.
         4. Each WRITE command may be to any bank.

Figure 27:   WRITE-to-READ – Uninterrupting

DON'T CARE   TRANSITIONING DATA

Notes: 1. D<small>IN</small> *b* = data-in for column *b*; D<small>OUT</small> *n* = data-out for column *n*.
2. An uninterrupted burst of 4 is shown.
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case ^{t}WTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 28: WRITE-to-READ – Interrupting
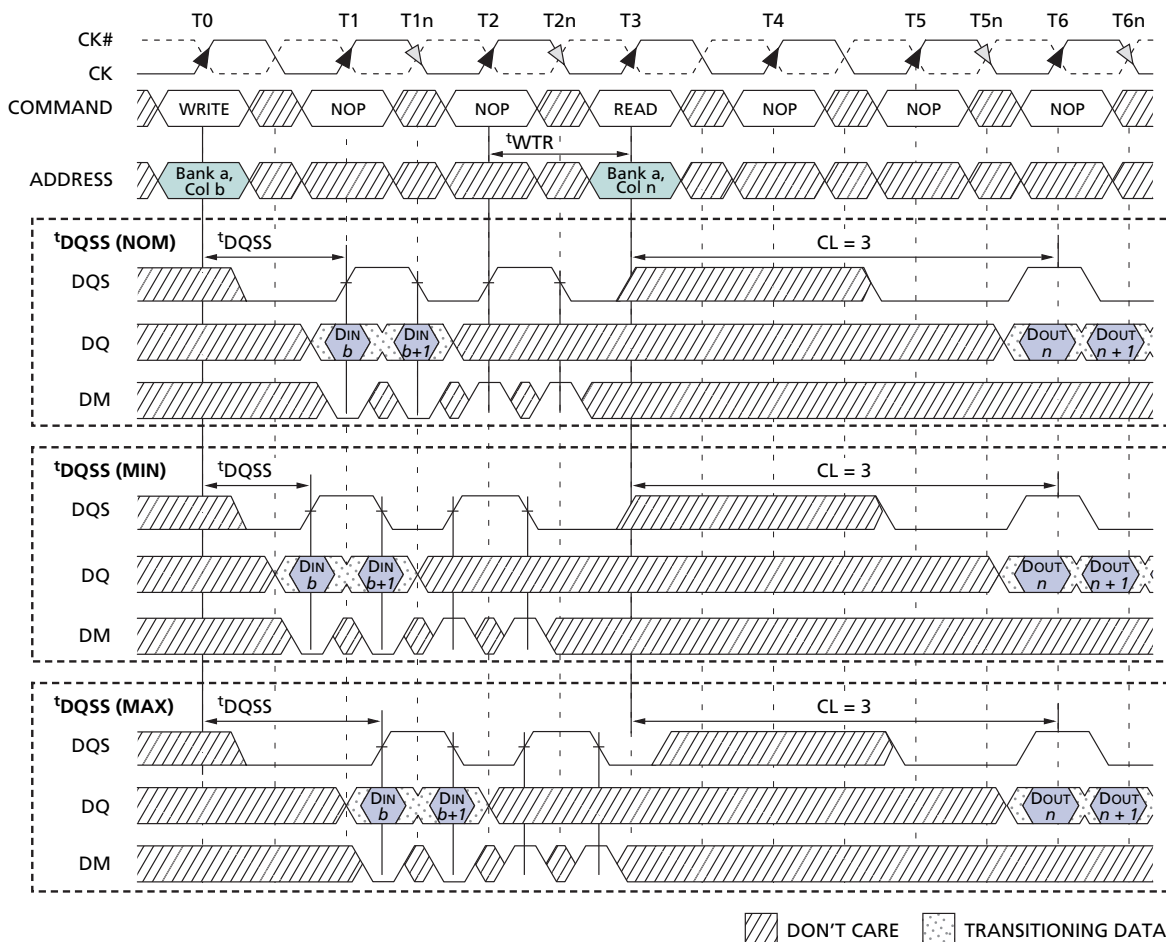
DON'T CARE   TRANSITIONING DATA

Notes:
1. D$_{IN}$ b = data-in for column b; D$_{OUT}$ n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written.
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

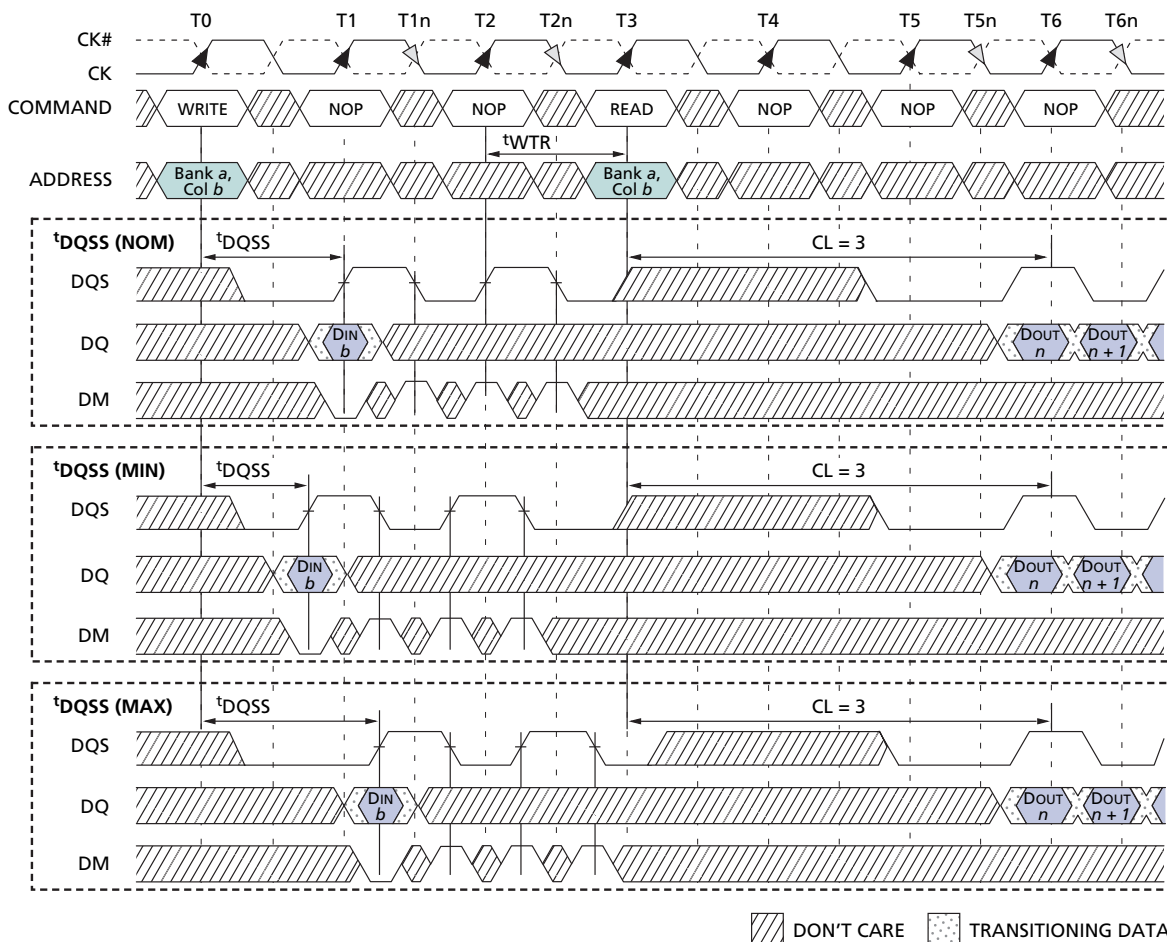**Figure 29:   WRITE-to-READ – Odd Number of Data, Interrupting**

Notes: 1. D$_{IN}$ *b* = data-in for column *b*; D$_{OUT}$ *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; one data elements is written, three are masked.
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T2n, T3, and T3n because the READ command would not mask these three data elements.

Figure 30: WRITE-to-PRECHARGE – Uninterrupting

| DON'T CARE | TRANSITIONING DATA |
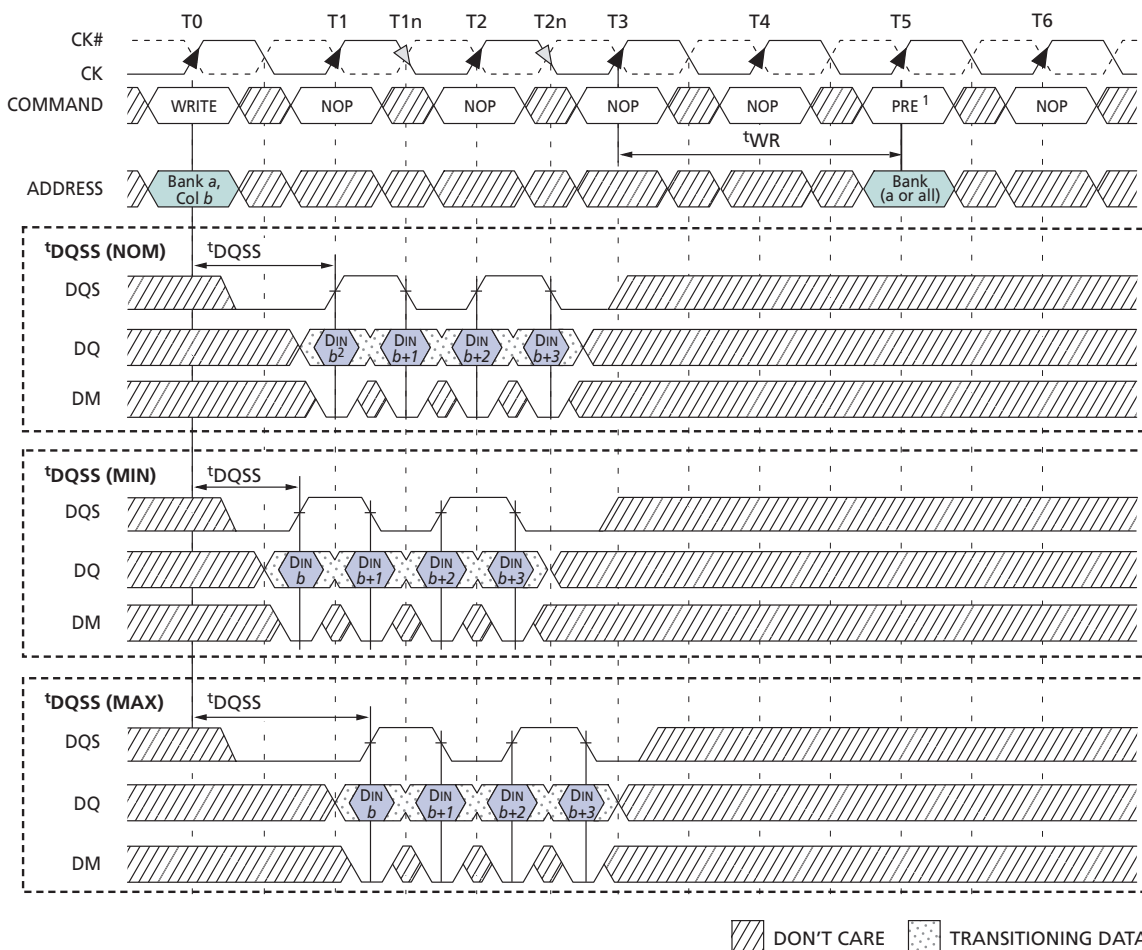
Notes: 1. PRE = PRECHARGE command.
2. DIN b = data-in for column b.
3. An unterrupted burst 4 of is shown.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. tWR is referenced from the first positive CK edge after the last data-in pair.
6. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices; in this case, tWR is not required and the PRECHARGE command could be applied earlier.

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Figure 31: WRITE-to-PRECHARGE – Interrupting
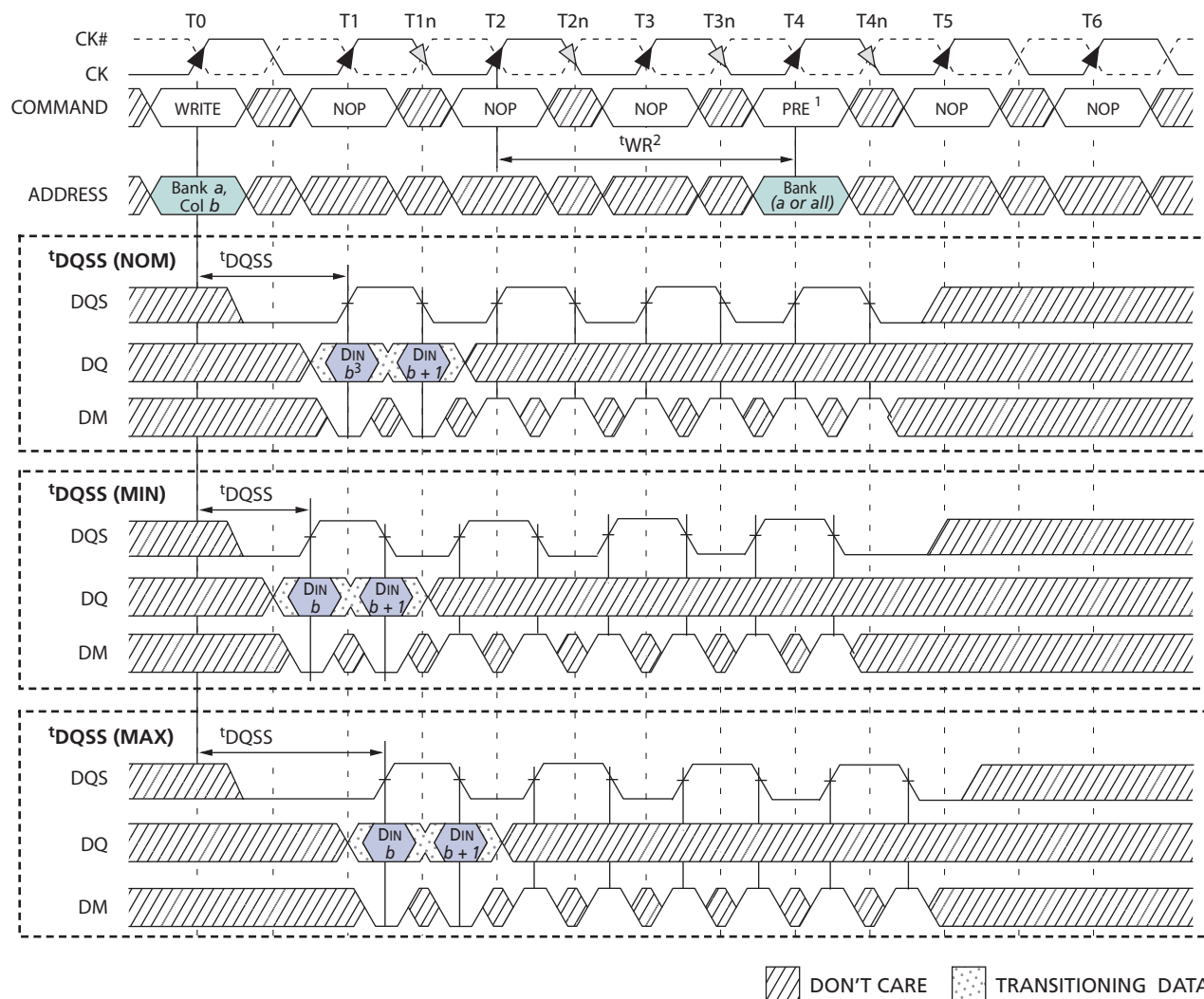
Notes:
1. PRE = PRECHARGE command.
2. ^tWR is referenced from the first positive CK edge after the last data-in pair.
3. D$_{IN}$ b = data-in for column b.
4. An interrupted burst of 8 is shown; two data elements are written.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T4 and T4n to register DM.
7. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

Figure 32: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting
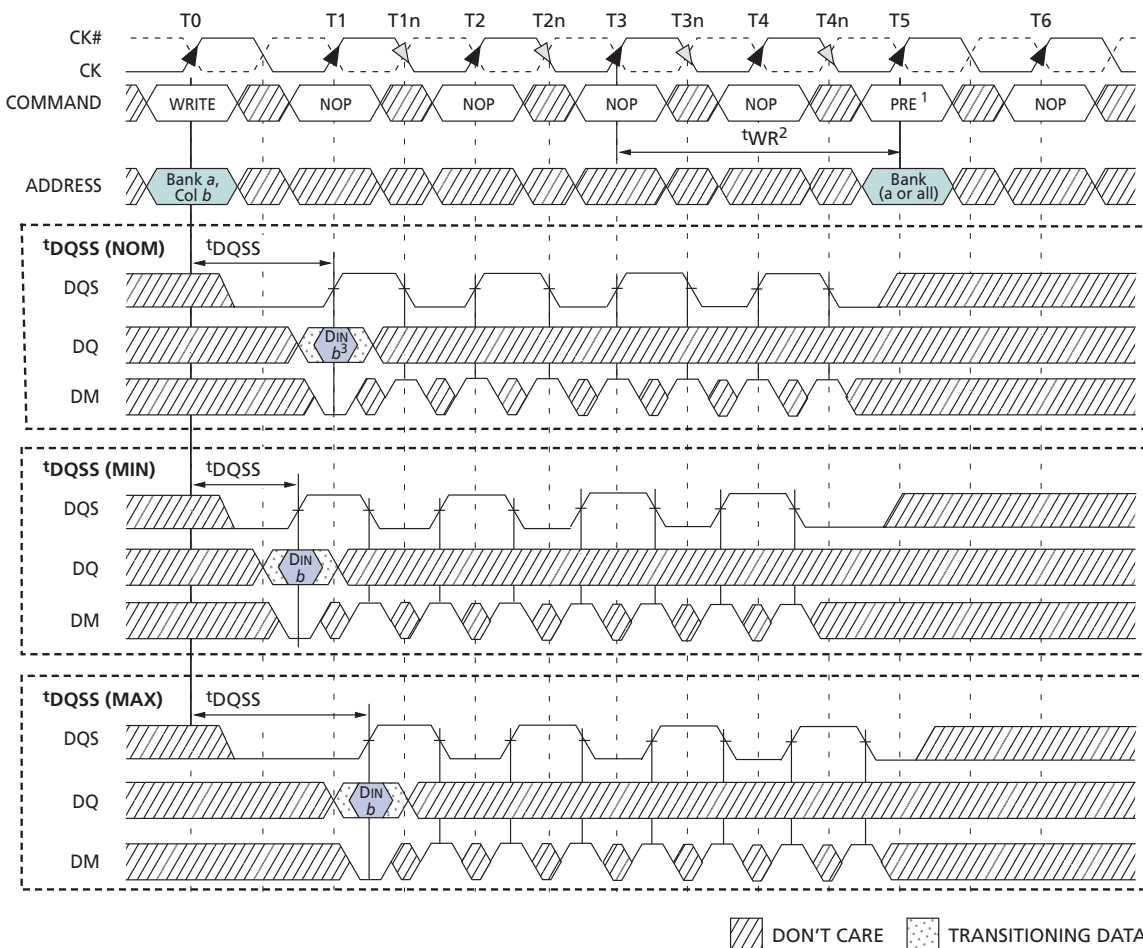
Notes: 1. PRE = PRECHARGE command.
2. t_{WR} is referenced from the first positive CK edge after the last data-in pair.
3. D_{IN} b = data-in for column b.
4. An interrupted burst of 8 is shown; one data element is written.
5. DQS is required at T4 and T4n to register DM.
6. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.
7. A10 is LOW with the WRITE command (auto precharge is disabled).

PRECHARGE Command

The PRECHARGE command (Figure 33) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged (A10 = LOW), inputs BA0, BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0, BA1 are treated as a "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 33: PRECHARGE Command
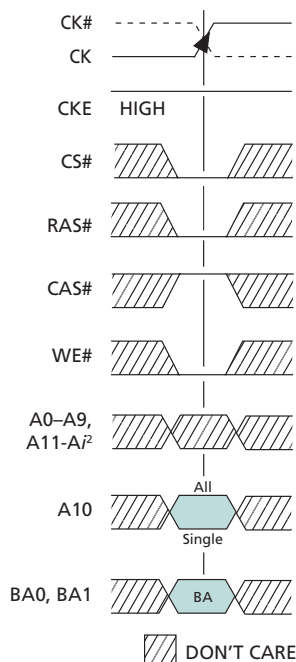
Notes: 1. BA = bank address.
All = A10 HIGH, all banks to be precharged, BA1, BA0 are "Don't Care."
Single = A10 LOW, only bank selected by BA1 and BA0 will be precharged.
2. i = the most significant column address bit for each configuration.

Power-Down

Power-down (Figure 33) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates all input and output buffers, including CK and CK# and excluding CKE. Exiting power-down requires the device to be at the same voltage as when it entered power-down and receiving a stable clock.

Note: The power-down duration is limited by the refresh requirements of the device.

While in power-down, CKE LOW must be maintained at the inputs of the Mobile DDR SDRAM, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT

command). NOPs or DESELECT commands must be maintained on the command bus until ^{t}XP is satisfied. See Figure 43 on page 70 for a detailed illustration of the power-down command.

Figure 34:   Power-Down Command (in Active or Precharge Modes)

DON'T CARE
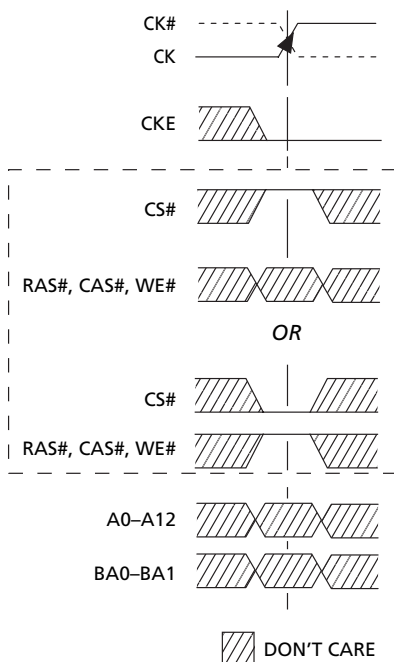
Deep Power-Down (DPD)

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained once the device enters deep power-down mode.

Before entering DPD mode the DRAM must be in all banks idle state with no activity on the data bus (^{t}RP time must be met). This mode is entered by holding CS# and WE# LOW with RAS# and CAS# HIGH at the rising edge of the clock while CKE is LOW. CKE must be held LOW to maintain DPD mode. The clock must be stable prior to exiting DPD mode. This mode is exited by asserting CKE HIGH with either a NOP or DESELECT command present on the command bus. Upon exiting DPD mode, 200μs of valid clocks with either NOPs or DESELECT commands present on the command bus are required; a PRECHARGE ALL command and a full DRAM initialization sequence are required.

Figure 35:   Deep Power-Down Command
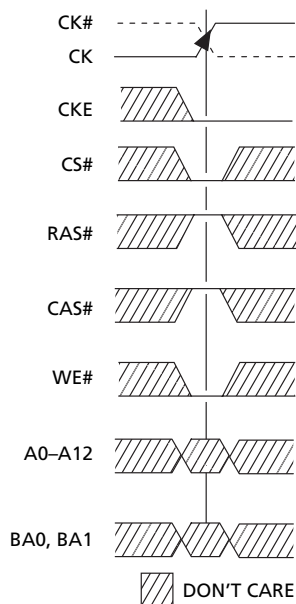
Figure 36:   Deep Power-Down
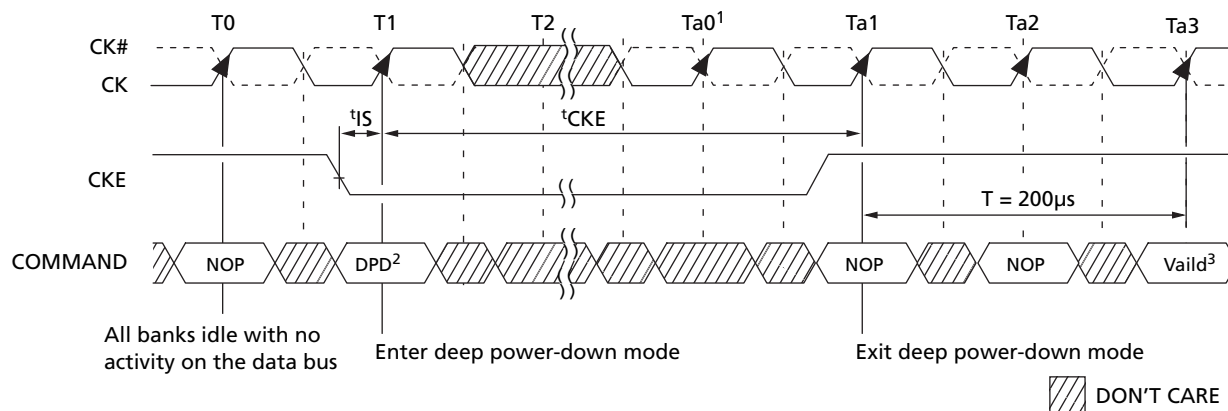
Notes: 1. Clock must be stable prior to CKE going HIGH.
2. DPD = Deep power-down mode command.
3. Upon exit of deep power-down mode, a PRECHARGE ALL command must be issued fol-
lowed by the initialization sequence (page 14).

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Table 8: Truth Table – CKE

Notes: 1–5

CKE$_{n-1}$	CKE$_n$	Current State	COMMAND$_n$	ACTION$_n$	Notes
L	L	Active power-down	X	Maintain active power-down	
L	L	Deep power-down	X	Maintain deep power-down	
L	L	(Precharge) power-down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	Active power-down	DESELECT or NOP	Exit active power-down	6, 7
L	H	Deep power-down	DESELECT or NOP	Exit deep power-down	10, 11
L	H	(Precharge) power-down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	Active power-down entry	
H	L	All banks idle	BURST TERMINATE	Deep power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 10 on page 52		
H	H		See Table 10 on page 52		

Notes:
1. CKE$_n$ is the logic state of CKE at clock edge n; CKE$_{n-1}$ was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMAND$_n$ is the command registered at clock edge n, and ACTION$_n$ is a result of COMMAND$_n$.
4. All states and sequences not shown are illegal or reserved.
5. ^{t}CKE pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the ^{t}XP period.
7. The clock must toggle at least one time during the ^{t}XP period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the ^{t}XSR period.
9. The clock must toggle at least one time during the ^{t}XSR period.
10. 200µs of valid clocks and NOPs (or DESELECTs) commands are required before any other valid command is allowed.
11. Upon exiting deep power-down mode and after the 200µs, a PRECHARGE ALL command is required, followed by the standard initialization sequence.

Table 9: Truth Table – Current State Bank *n* - Command to Bank *n*
Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11
	L	H	H	L	BURST TERMINATE	9

Notes: 1. This table applies when CKE$_{n-1}$ was HIGH and CKE$_n$ is HIGH and after ^{t}XSR has been met (if the previous state was self refresh), after ^{t}XP has been met (if the previous state was power down), or 200μs if the previous state was deep power-down).

2. This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.

3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to any other bank are determined by that bank's current state.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the row active state.

   Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

   Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR SDRAM will be in the all banks idle state.

Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the Mobile DDR SDRAM will be in the all banks idle state.

Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 10:   Truth Table – Current State Bank *n* – Command to Bank *m*

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes: 1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH and after ^tXSR has been met (if the previous state was self refresh) or after ^tXP has been met (if the previous state was power-down).

2. This table describes alternate bank operation, except where noted (for example, the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions:

Idle:	The bank has been precharged, and ^tRP has been met.
Row active:	A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

3a. The read with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^tWR ends, with ^tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^tRP) begins.

This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized below.

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP WRITE or WRITE w/AP PRECHARGE ACTIVE	$[1 + (BL/2)] \, {}^tCK + {}^tWTR$ $(BL/2) \, {}^tCK$ $1 \, {}^tCK$ $1 \, {}^tCK$
READ w/AP	READ or READ w/AP WRITE or WRITE w/AP PRECHARGE ACTIVE	$(BL/2) \times {}^tCK$ $[CL_{RU} + (BL/2)] \, {}^tCK$ $1 \, {}^tCK$ $1 \, {}^tCK$

CL_{RU} = CL rounded up to the next integer.

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Electrical Specifications

Table 11:   Operating Temperature

Parameter	Symbol	Min	Max	Unit	Notes
Operating temperature					
T_A (commercial		0	+70	°C	
T_A (industrial)	IT	−40	+85	°C	
Storage temperature (plastic)	T_{STG}	−55	+150	°C	

Table 12:   AC/DC Electrical Characteristics and Operating Conditions
Notes: 1–5; notes appear on page 61
V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	1.70	1.95	V	32, 34
I/O supply voltage	V_{DDQ}	1.70	1.95	V	32, 34
Address and command inputs					
Input voltage high	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	25, 33
Input voltage low	V_{IL}	−0.3	0.2 × V_{DDQ}	V	25, 33
Clock Inputs (CK, CK#)					
DC input voltage	V_{IN}	−0.3	V_{DDQ} + 0.3	V	27
DC input differential voltage	$V_{ID}(DC)$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	8, 27
AC input differential voltage	$V_{ID}(AC)$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	8, 27
AC differential crossing voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	9, 27
Data inputs					
DC input high voltage	$V_{IH}(DC)$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	25, 28, 33
AC input high voltage	$V_{IH}(AC)$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	25, 28, 33
DC input low voltage	$V_{IL}(DC)$	−0.3	0.3 × V_{DDQ}	V	25, 28, 33
AC input low voltage	$V_{IL}(AC)$	−0.3	0.2 × V_{DDQ}		25, 28, 33
Data outputs					
DC output high voltage: Logic 1 (I_{OH} = −0.1mA)	V_{OH}	0.9 × V_{DDQ}	−	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	−	0.1 × V_{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	−1	1	µA	
Output leakage current (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	−5	5	µA	

Table 13:   Capacitance (x16, x32)

Notes: 13; notes appear on page 61

Parameter	Symbol	Min	Max	Unit	Notes
Delta input/output capacitance: DQs, DQS, DM	DC_{I0}	–	2.0	pF	21
Delta input capacitance: command and address	DC_{I1}	–	2.25	pF	26
Delta input capacitance: CK, CK#	DC_{I2}	–	0.5	pF	26
Input/output capacitance: DQs, DQS, DM	C_{I0}	2.0	5.0	pF	
Input capacitance: command and address	C_{I1}	2.0	5.0	pF	
Input capacitance: CK, CK#	C_{I2}	2.0	3.5	pF	
Input capacitance: CS#, CKE	C_{I3}	2.0	5.0	pF	

Table 14: I$_{DD}$ Specifications and Conditions (x16)

Notes: 1–5, 10, 12, 14; notes appear on page 61; V$_{DD}$/V$_{DDQ}$ = 1.70–1.95V

Parameter/Condition	Symbol	Max -6	Max -75	Unit	Notes
Operating one bank active-precharge current: ^{t}RC = ^{t}RC (MIN); ^{t}CK = ^{t}CK (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable	I$_{DD0}$	95	90	mA	19
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH, ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD2P}$	600	600	µA	20, 29, 44
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	I$_{DD2PS}$	600	600	µA	20, 29, 44
Precharge nonpower-down standby current: All banks idle CKE = HIGH; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD2N}$	36	30	mA	36
Precharge nonpower-down standby current: Clock stopped All banks idle, CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH Address and control inputs are switching; Data bus inputs are stable	I$_{DD2NS}$	24	18	mA	36
Active power-down standby current: One bank active, CKE = LOW; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD3P}$	3.6	3.6	mA	20, 29
Active power-down standby current: clock stopped One bank active, CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	I$_{DD3PS}$	3.6	3.6	mA	20, 29
Active nonpower-down standby: One bank active, CKE = HIGH; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD3N}$	36	30	mA	19
Active nonpower-down standby: Clock stopped One bank active, CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH Address and control inputs are switching; Data bus inputs are stable	I$_{DD3NS}$	30	24	mA	19
Operating burst read: One bank active; BL = 4; ^{t}CK = ^{t}CK (MIN); continuous read bursts; I$_{OUT}$ = 0mA; Address inputs are switching every two clock cycles; 50% data changing each burst	I$_{DD4R}$	140	130	mA	19
Operating burst write: One bank active; BL = 4; ^{t}CK = ^{t}CK (MIN); continuous WRITE bursts; Address inputs are switching; 50% data changing each burst	I$_{DD4W}$	140	130	mA	19
Auto refresh: ^{t}RFC = ^{t}RFC (MIN)	I$_{DD5}$	190	175	mA	37
Burst refresh; CKE = HIGH Address and control inputs are switching; Data bus inputs are stable ^{t}RFC = ^{t}REFI	I$_{DD5A}$	15	14	mA	24, 37
Deep power-down current: Address and control balls are stable; Data bus inputs are stable	I$_{DD8}$	10		µA	44, 45

Table 15:   I$_{DD}$ Specifications and Conditions (x32)
Notes: 1–5, 10, 12, 14; notes appear on pages 61
V$_{DD}$/V$_{DDQ}$ = 1.70–1.95V

Parameter/Condition	Symbol	Max -6	Max -75	Unit	Notes
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable	I$_{DD}$0	110	105	mA	19
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH, $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$2P	600	600	µA	20, 29, 44
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$2PS	600	600	µA	20, 29, 44
Precharge nonpower-down standby current: All banks idle CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$2N	36	30	mA	36
Precharge nonpower-down standby current: clock stopped All banks idle, CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$2NS	24	18	mA	36
Active power-down standby current: One bank active, CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$3P	3.6	3.6	mA	20, 29
Active power-down standby current: Clock stopped One bank active, CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$3PS	3.6	3.6	mA	20, 29
Active nonpower-down standby: One bank active, CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$3N	36	30	mA	19
Active nonpower-down standby: Clock stopped One bank active, CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH Address and control inputs are switching; Data bus inputs are stable	I$_{DD}$3NS	30	24	mA	19
Operating burst read: One bank active; BL = 4; CL = 3; $^tCK = {}^tCK$ (MIN); Continuous read bursts; I$_{OUT}$ = 0mA; Address inputs are switching every two clock cycles; 50% data changing each burst	I$_{DD}$4R	140	130	mA	19
Operating burst write: One bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst	I$_{DD}$4W	160	140	mA	19
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable $^tRFC = {}^tRFC$ (MIN)	I$_{DD}$5	190	175	mA	37
$^tRFC = {}^tREFI$	I$_{DD}$5A	15	14	mA	24, 37
Deep power-down current: Address and control pins are stable; Data bus inputs are stable	I$_{DD}$8	10	10	µA	44, 45

Table 16: I_{DD}6 Specifications and Conditions (x32)
Notes: 1–5, 10–12, 14; notes appear on pages 61; V_{DD}/V_{DD}Q = 1.70–1.95V

Parameter/Condition		Symbol	Max -75/-8	Units
Self refresh CKE = LOW; ^{t}CK = ^{t}CK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 85°C	I_{DD}6A	900	µA
	Full array, 70°C	I_{DD}6B	720	µA
	Full array, 45°C	I_{DD}6C	360	µA
	Full array, 15°C	I_{DD}6D	270	µA
	Half array, 85°C	I_{DD}6A	585	µA
	Half array, 70°C	I_{DD}6B	495	µA
	Half array, 45°C	I_{DD}6C	315	µA
	Half array, 15°C	I_{DD}6D	225	µA
	1/4 array, 85°C	I_{DD}6A	405	µA
	1/4 array, 70°C	I_{DD}6B	315	µA
	1/4 array, 45°C	I_{DD}6C	225	µA
	1/4array, 15°C	I_{DD}6D	180	µA
	1/8 array, 85°C	I_{DD}6A	360	µA
	1/8 array, 70°C	I_{DD}6B	315	µA
	1/8 array, 45°C	I_{DD}6C	180	µA
	1/8 array, 15°C	I_{DD}6D	158	µA
	1/16 array, 85°C	I_{DD}6A	315	µA
	1/16 array, 70°C	I_{DD}6B	270	µA
	1/16 array, 45°C	I_{DD}6C	180	µA
	1/16 array, 15°C	I_{DD}6D	158	µA

Figure 37: Typical Self Refresh Current vs. Temperature

TBD

Table 17:   Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–6, 27; notes appear on pages 61
V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter		Symbol	-6		-75		Unit	Notes
			Min	Max	Min	Max		
Access window of DQs from CK/CK#	CL = 3	^tAC	2.0	5.5	2.0	6.0	ns	7
	CL = 2	^tAC	2.0	6.5	2.0	6.5	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	^tCK	
CK low-level width		^tCL	0.45	0.55	0.45	0.55	^tCK	
Clock cycle time	CL = 3	$^tCK(3)$	6	–	7.5	–	ns	7
	CL = 2	$^tCK(2)$	12	–	12	–	ns	
Minimum ^tCKE HIGH/LOW time		^tCKE	1	–	1	–	^tCK	
Auto precharge write recovery + precharge time		^tDAL	–	–	–	–		40
DQ and DM input hold time relative to DQS		^tDH	0.5	–	0.75	–	ns	23, 28, 39
DQ and DM input setup time relative to DQS		^tDS	0.5	–	0.75	–	ns	
DQ and DM input pulse width (for each input)		^tDIPW	2.1	–	2.2	–	ns	41
Access window of DQS from CK/CK#	CL = 3	^tDQSCK	2.0	5.5	2.0	6.0	ns	7
	CL = 2	^tDQSCK	2.0	6.5	2.0	6.5	ns	
DQS input high pulse width		^tDQSH	0.35	0.6	0.4	0.6	^tCK	
DQS input low pulse width		^tDQSL	0.35	0.6	0.4	0.6	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.45	–	0.6	ns	22, 23
WRITE command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	0.2	–	^tCK	
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	0.2	–	^tCK	
Data valid output window (DVW)		n/a	^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	22
Half-clock period		^tHP	$^tCH, ^tCL$	–	$^tCH, ^tCL$	–	ns	30
Data–out High-Z window from CK/CK#	CL = 3	^tHZ	–	5.5	–	6.0	ns	7, 15, 35, 36
	CL = 2		–	6.5	–	6.5	ns	
Data-out Low-Z window from CK/CK#		^tLZ	1.0	–	1.0	–	ns	15, 36
Address and control input hold time (fast slew rate)		^tIH_F	1.1	–	1.3	–	ns	14, 39
Address and control input setup time (fast slew rate)		^tIS_F	1.1	–	1.3	–	ns	14, 39
Address and control input hold time (slow slew rate)		^tIH_S	1.2	–	1.5	–	ns	14, 39
Address and control input setup time (slow slew rate)		^tIS_S	1.2	–	1.5	–	ns	14, 39
Address and control input pulse width		^tIPW	2.7	–	3.0	–	ns	41
LOAD MODE REGISTER command cycle time		^tMRD	2	–	2	–	^tCK	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	^tHP -^tQHS	–	ns	22, 23
Data hold skew factor		^tQHS	–	0.65	–	0.75	ns	
ACTIVE-to-PRECHARGE command		^tRAS	42	70,000	45	70,000	ns	31
ACTIVE-to-ACTIVE/ACTIVE-to-AUTO REFRESH command period		^tRC	60	–	75	–	ns	
AUTO REFRESH command period		^tRFC	140	–	140	–	ns	37

Table 17: Electrical Characteristics and Recommended AC Operating Conditions (continued)
Notes: 1–6, 27; notes appear on pages 61
VDD/VDDQ = 1.70–1.95V

Parameter		Symbol	-6 Min	-6 Max	-75 Min	-75 Max	Unit	Notes
ACTIVE to READ or WRITE delay		^tRCD	18		22.5		ns	
Refresh period		^tREF	–	64	–	64	ms	
Average periodic refresh interval		^tREFI	–	7.8	–	7.8	µs	20
PRECHARGE command period		^tRP	18	–	22.5	–	ns	
DQS read preamble	CL = 2	^tRPRE(2)	0.5	1.1	0.5	1.1	^tCK	
DQS read preamble	CL = 3	^tRPRE(3)	0.9	1.1	0.9	1.1	^tCK	
DQS read postamble		^tRPST	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank a to ACTIVE bank b command		^tRRD	12	–	15	–	ns	
Read of SRR to next valid command		^tSRC	CL + 1	–	CL + 1	–	^tCK	
SRR to READ		^tSRR	2	–	2	–	^tCK	
DQS write preamble		^tWPRE	0.25	–	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	0	–	ns	17, 18
DQS write postamble		^tWPST	0.4	0.6	0.4	0.6	^tCK	16
Write recovery time		^tWR	15	–	15	–	ns	46
Internal WRITE to READ command delay		^tWTR	1	–	1	–	^tCK	
Exit SELF REFRESH to first valid command		^tXSR	140	–	140	–	ns	42
Exit power-down mode to first valid command		^tXP	1	–	1	–	^tCK	43

Notes

1. All voltages referenced to V_{SS}.

2. All parameters assume proper device initialization.

3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:
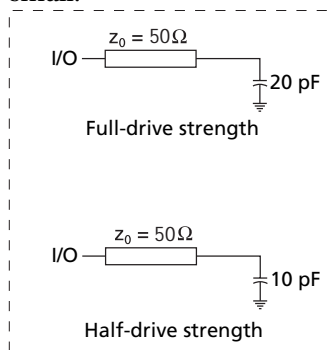
5. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ}/2$.

6. All AC timings assume an input slew rate of 1 V/ns.

7. CAS latency definition: with CL = 2 the first data element is valid at $(^tCK + {}^tAC)$ after the clock at which the READ command was registered, for CL = 3 the first data element is valid at $(2 \times {}^tCK + {}^tAC)$ after the first clock at which the READ command was registered.

8. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

9. The value of V_{IX} is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.

10. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 with the outputs open.

11. Enables on-die refresh and address counters.

12. I_{DD} specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.

13. This parameter is sampled. V_{DD}/V_{DDQ} = 1.70–1.95V, f = 100 MHz, T_A = 25°C, $V_{OUT(DC)}$ = $V_{DDQ}/2$, V_{OUT} (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

14. Fast command/address input slew rate ≥1 V/ns. Slow command/address input slew rate ≥0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: ^tIS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. ^tIH remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.

15. ^tHZ and ^tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

17. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.

18. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.

19. MIN (^{t}RC or ^{t}RFC) for I$_{DD}$ measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I$_{DD}$ measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

20. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.

21. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

22. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}HP – ^{t}QHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.

23. Referenced to each output group: For x16, LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15. For x32, DQS0 with DQ0–DQ7; DQS1 with DQ8–DQ15; DQS2 with DQ16–DQ23; and DQS3 with DQ24–DQ31.

24. This limit is actually a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (for example, during standby).

25. To maintain a valid level, the transitioning edge of the input must:
Sustain a constant slew rate from the current AC level through to the target AC level, V$_{IL}$(AC) or V$_{IH}$(AC).

   25a. Reach at least the target AC level.

   25b. After the AC target level is reached, continue to maintain at least the target DC level, V$_{IL}$(DC) or V$_{IH}$(DC).

26. The input capacitance per pin group will not differ by more than this maximum amount for any given device.

27. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).

28. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

29. V$_{DD}$ must not vary more than 4% if CKE is not active while any bank is active.

30. ^{t}HP (MIN) is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK# inputs, collectively.

31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.

32. Any positive glitch must be less than 1/3 of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –150mV or 1.6V, whichever is more positive.

33. V$_{IH}$ overshoot: V$_{IH}$ (MAX) = V$_{DDQ}$ + 1.0V for a pulse width ≤3ns and the pulse width cannot be greater than 1/3 of the cycle rate. V$_{IL}$ undershoot: V$_{IL}$ (MIN) = –1.0V for a pulse width ≤3ns and the pulse width can not be greater than 1/3 of the cycle rate.

34. V$_{DD}$ and V$_{DDQ}$ must track each other and V$_{DDQ}$ must be less than or equal to V$_{DD}$.

35. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.

36. I$_{DD2N}$ specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.

37. CKE must be active (HIGH) during the entire time a refresh command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC later.

38. The values for I$_{DD}$6 at 70°C, 45°C, and 15°C are approximate only and are not tested.

39. The transition time for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between V$_{IL}$(DC) to V$_{IH}$(AC) for rising input signals and V$_{IH}$(DC) to V$_{IL}$(AC) for falling input signals.

40. ^{t}DAL = (^{t}WR/^{t}CK) + (^{t}RP/^{t}CK): for each term, if not already an integer, round to the next higher integer.

41. These parameters guarantee device timing but are not tested on each device.

42. Clock must be toggled a minimum of two times during this period.

43. Clock must be toggled a minimum of one time during this period.

44. Measurement is taken 500ms after entering into this operating mode to allow settling time for the tester.

45. Typical values at 25°C, not a maximum value.

46. At least one clock cycle is required during ^{t}WR time when in auto precharge mode.

Table 18:   Target Normal Output Drive Characteristics (Full-Drive Strength)
The above characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	−2.80	−18.53
0.20	5.60	26.80	−5.60	−26.80
0.30	8.40	32.80	−8.40	−32.80
0.40	11.20	37.05	−11.20	−37.05
0.50	14.00	40.00	−14.00	−40.00
0.60	16.80	42.50	−16.80	−42.50
0.70	19.60	44.57	−19.60	−44.57
0.80	22.40	46.50	−22.40	−46.50
0.85	23.80	47.48	−23.80	−47.48
0.90	23.80	48.50	−23.80	−48.50
0.95	23.80	49.40	−23.80	−49.40
1.00	23.80	50.05	−23.80	−50.05
1.10	23.80	51.35	−23.80	−51.35
1.20	23.80	52.65	−23.80	−52.65
1.30	23.80	53.95	−23.80	−53.95
1.40	23.80	55.25	−23.80	−55.25
1.50	23.80	56.55	−23.80	−56.55
1.60	23.80	57.85	−23.80	−57.85
1.70	23.80	59.15	−23.80	−59.15
1.80	–	60.45	–	−60.45
1.90	–	61.75	–	−61.75

Table 19:   Target Reduced Output Drive Characteristics (One-Half Drive Strength)

The above characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	−1.27	−8.42
0.20	2.55	12.30	−2.55	−12.30
0.30	3.82	14.95	−3.82	−14.95
0.40	5.09	16.84	−5.09	−16.84
0.50	6.36	18.20	−6.36	−18.20
0.60	7.64	19.30	−7.64	−19.30
0.70	8.91	20.30	−8.91	−20.30
0.80	10.16	21.20	−10.16	−21.20
0.85	10.80	21.60	−10.80	−21.60
0.90	10.80	22.00	−10.80	−22.00
0.95	10.80	22.45	−10.80	−22.45
1.00	10.80	22.73	−10.80	−22.73
1.10	10.80	23.21	−10.80	−23.21
1.20	10.80	23.67	−10.80	−23.67
1.30	10.80	24.14	−10.80	−24.14
1.40	10.80	24.61	−10.80	−24.61
1.50	10.80	25.08	−10.80	−25.08
1.60	10.80	25.54	−10.80	−25.54
1.70	10.80	26.01	−10.80	−26.01
1.80	–	26.48	–	−26.48
1.90	–	26.95	–	−26.95

Timing Diagrams

Figure 38: Data Output Timing – ^tDQSQ, ^tQH, and Data Valid Window (x16)
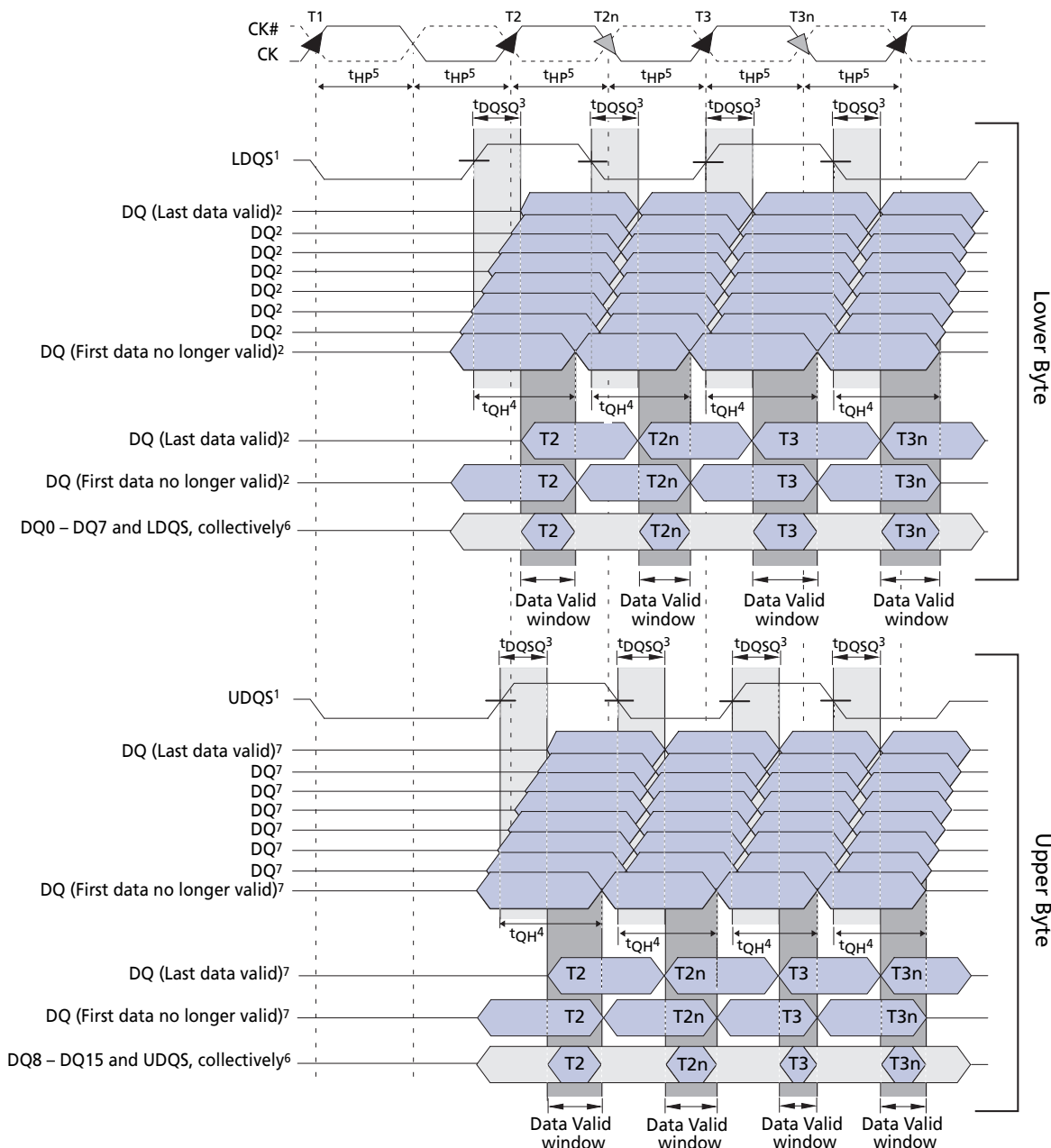
Notes: 1. DQ transitioning after DQS transitions define the ^tDQSQ window. LDQS defines the lower byte and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. ^tDQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. ^tQH is derived from ^tHP: $^tQH = {}^tHP - {}^tQHS$.
5. ^tHP is the lesser of ^tCL or ^tCH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transitions and is defined as $^tQH - {}^tDQSQ$.
7. DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.

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Figure 39:   Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window (x32)

Notes: 1. DQ transitioning after DQS transition define ^{t}DQS window. LDQS defines the lower byte and UDQS defines the upper byte.
2. Byte 0 is DQ0...7; Byte 1 is DQ8...15; Byte 2 is DQ16...23; Byte 3 is DQ24...31.
^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
3. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
4. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
5. The data valid window is derived for each DQS transition and is ^{t}QH - ^{t}DQSQ.

Figure 40: Data Output Timing – ^{t}AC and ^{t}DQSCK
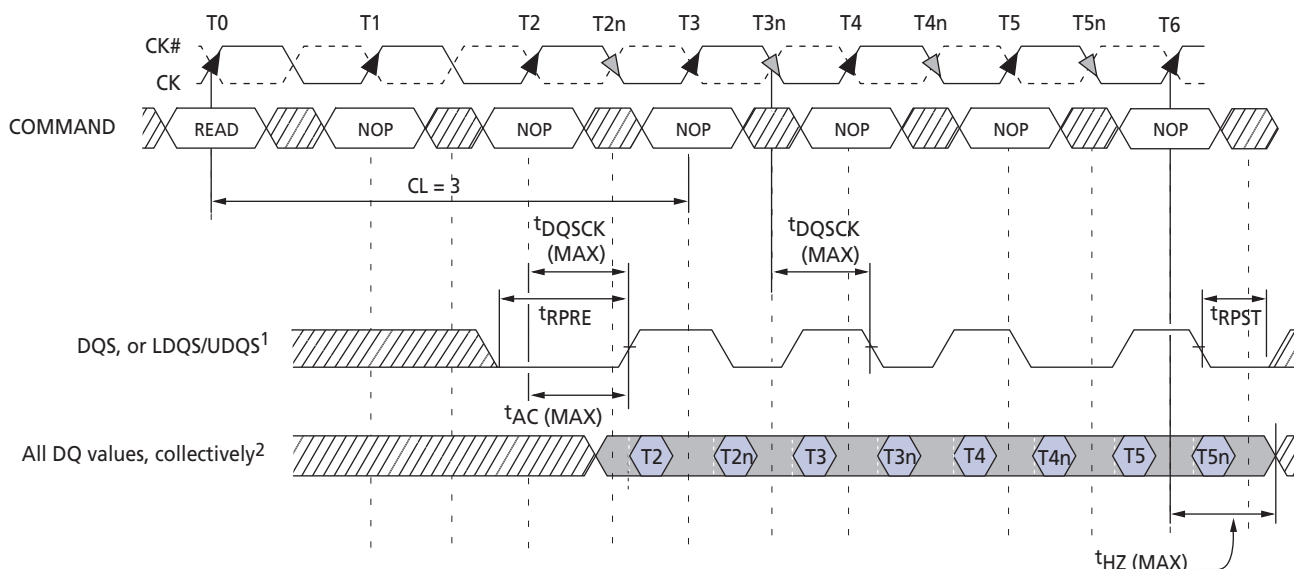
Notes: 1. DQ transitioning after DQS transition define ^{t}DQSQ window.
2. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
3. ^{t}AC is the DQ output window relative to CK and is the "long term" component of DQ skew.
4. Shown with CL = 3.

Figure 41: Data Input Timing

TRANSITIONING DATA   DON'T CARE
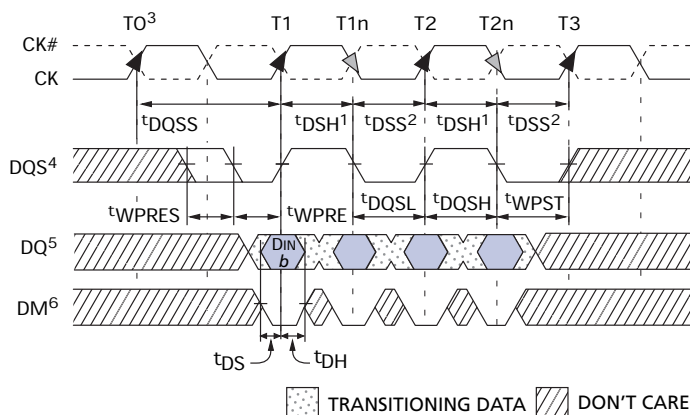
Notes: 1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. WRITE command issued at T0.
4. For x16, LDQS controls the lower byte; UDQS controls the upper byte.
5. For x32, DQS0 controls DQ[7:0], DQS1 controls DQ[15:8], DQS2 controls DQ[23:16], and DQS3 controls DQ[31:24].
6. For x16, LDM controls the lower byte; UDM controls the upper byte.
7. For x32, DM0 controls DQ[7:0], DM1 controls DQ[15:8], DM2 controls DQ[23:16], and DM3 controls DQ[31:24].

Figure 42: Initialize and Load Mode Registers
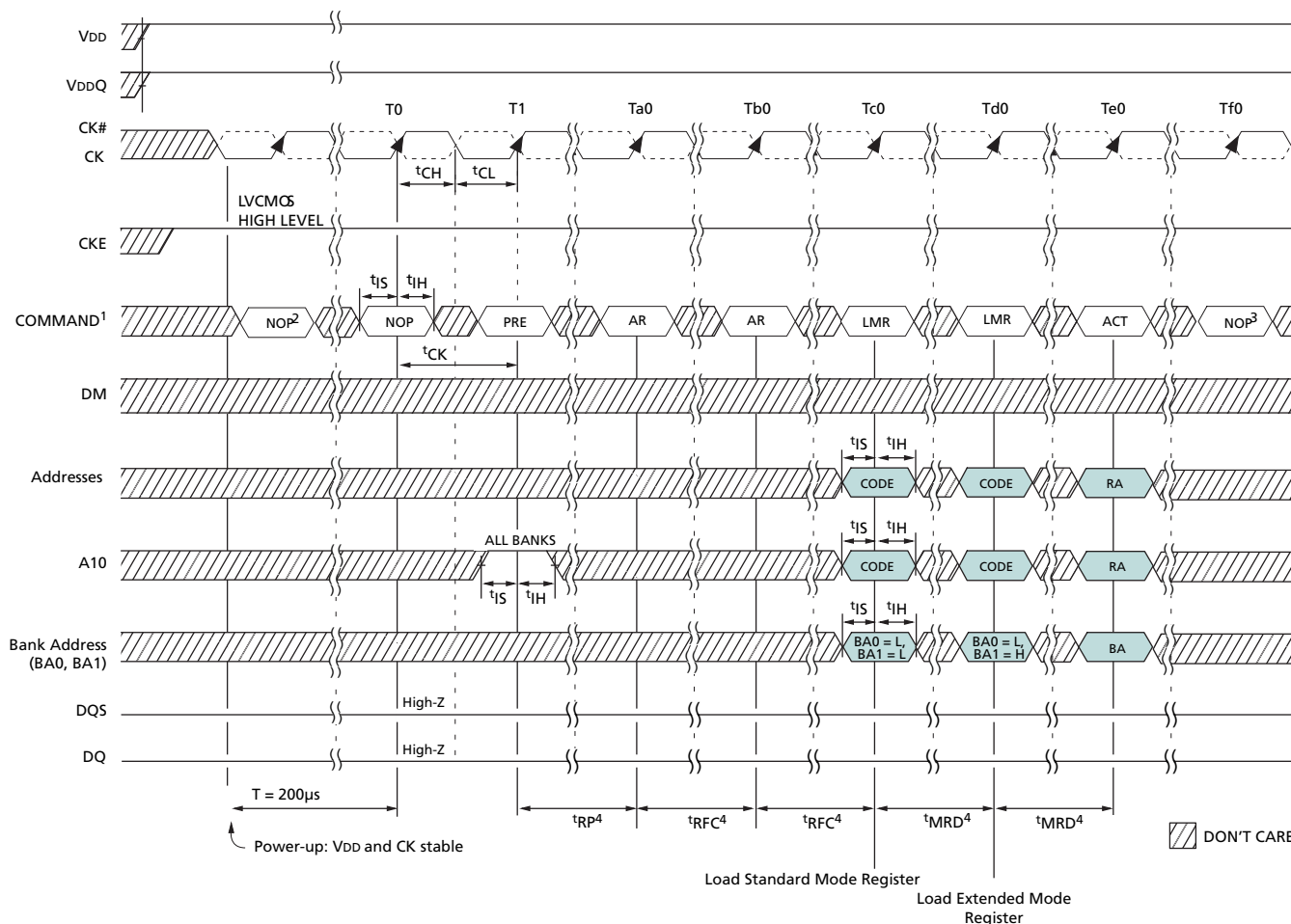
Notes: 1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command; RA = row address; BA = bank address.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

Figure 43: Power-Down Mode (Active or Precharge)
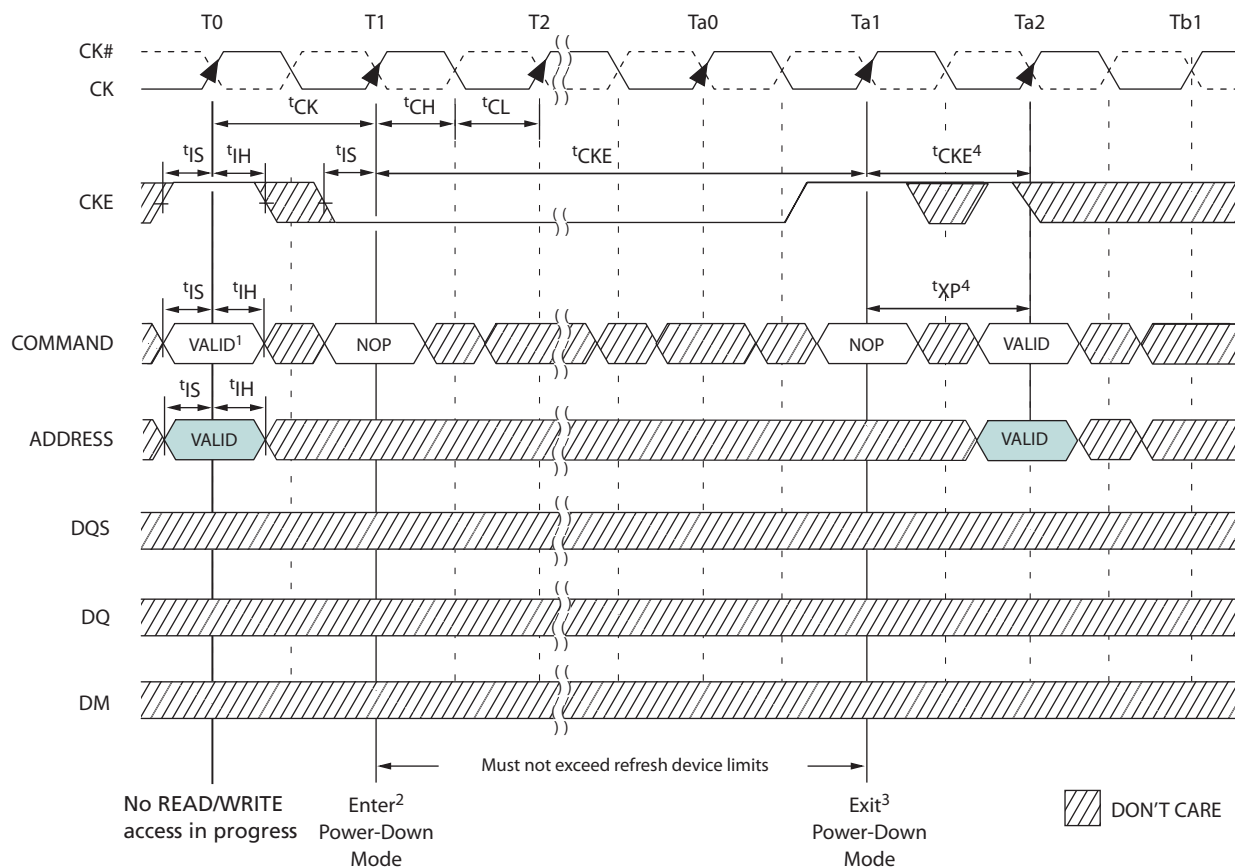
Notes: 1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during ^{t}XP time.
4. ^{t}CKE applies if CKE goes LOW at Ta2 (entering power-down); ^{t}XP applies if CKE remains HIGH at Ta2 (exit power-down).

Figure 44: Auto Refresh Mode
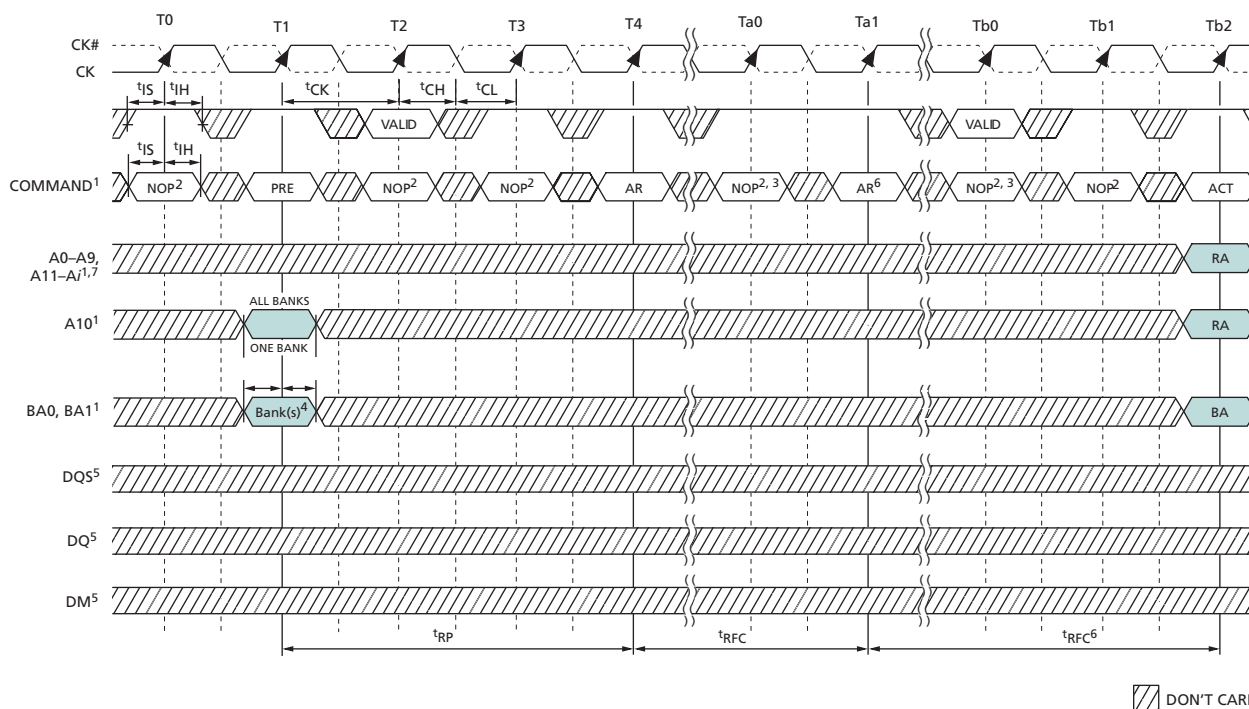
Notes:
1. PRE = PRECHARGE; ACT = ACTIVE; AR = AUTO REFRESH; RA = row address; BA = bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after t_{RFC} time; CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (for example, must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.
7. i = the most significant column address bit for each configuration.

Figure 45: Self Refresh Mode

DON'T CARE
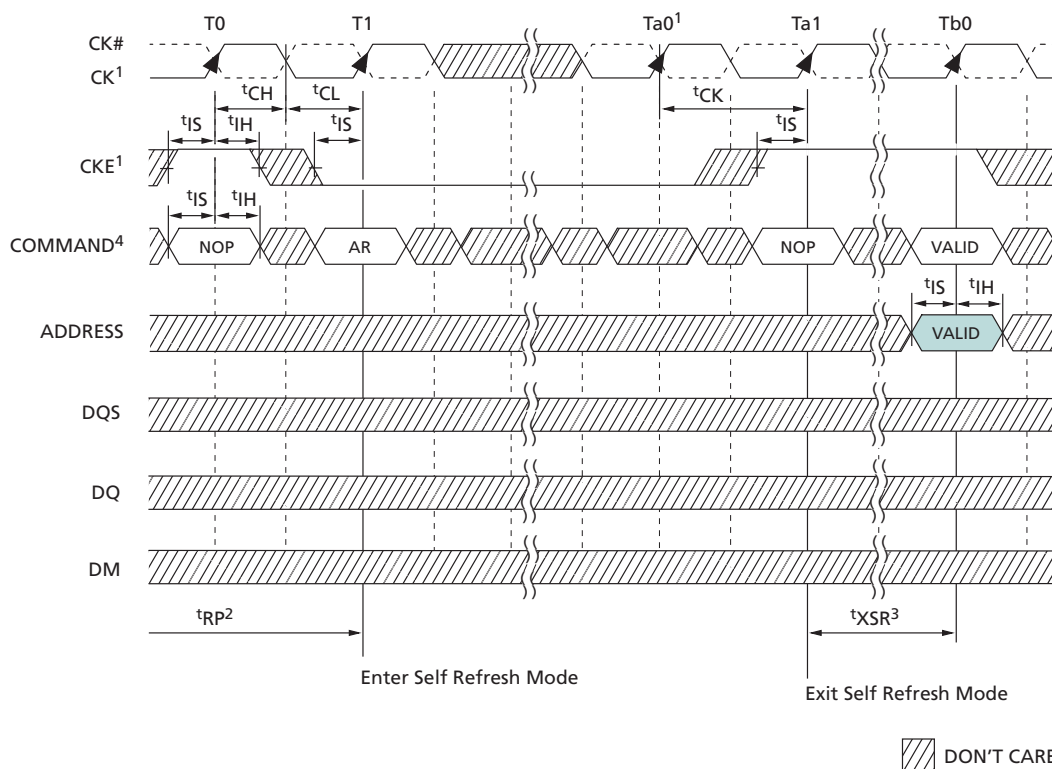
Notes: 1. Clock must be stable, cycling within specifications by Ta0, before exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT are required for ^{t}XSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.
5. CKE must remain LOW to remain in self refresh.
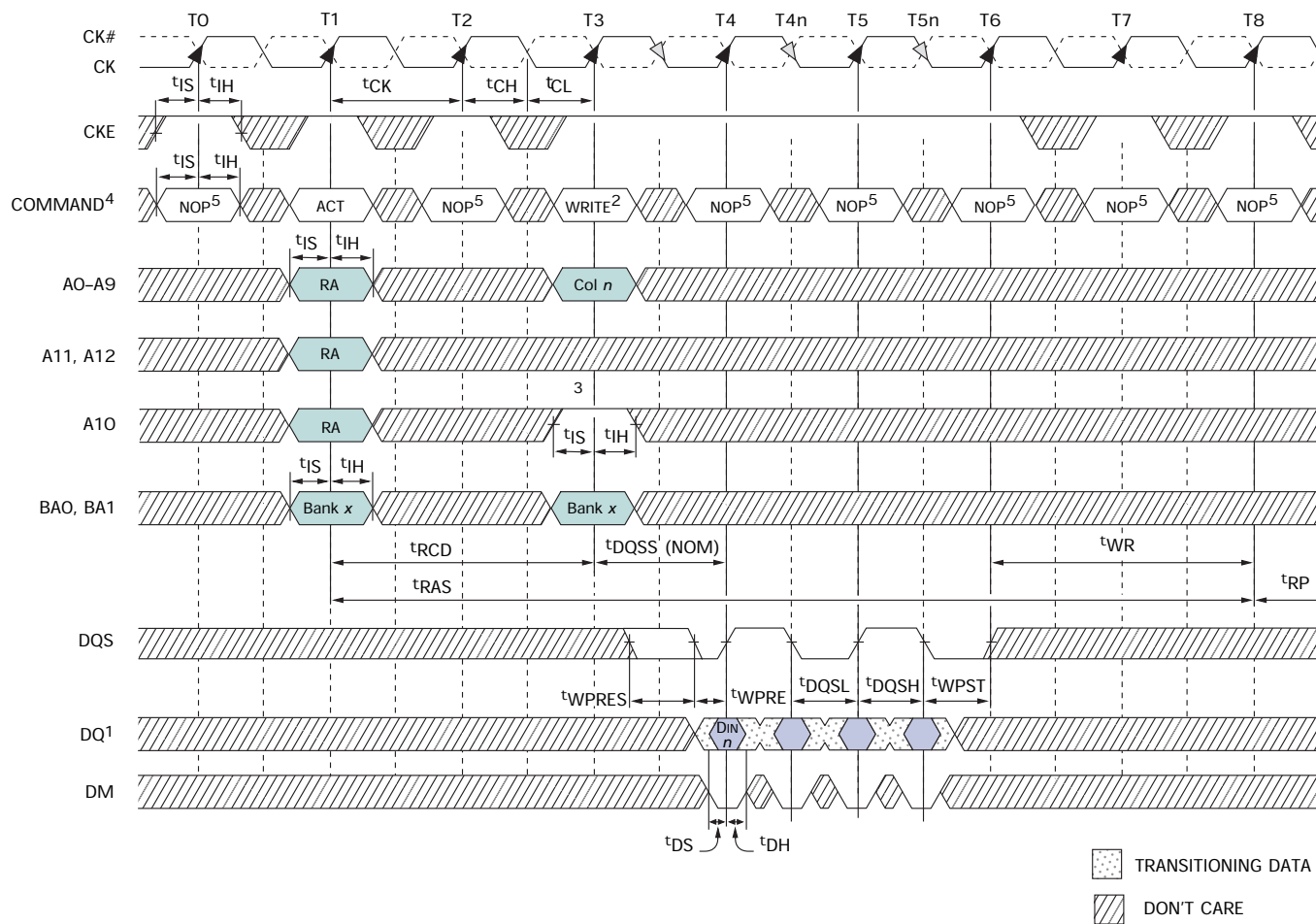
Figure 46: Bank Read – Without Auto Precharge
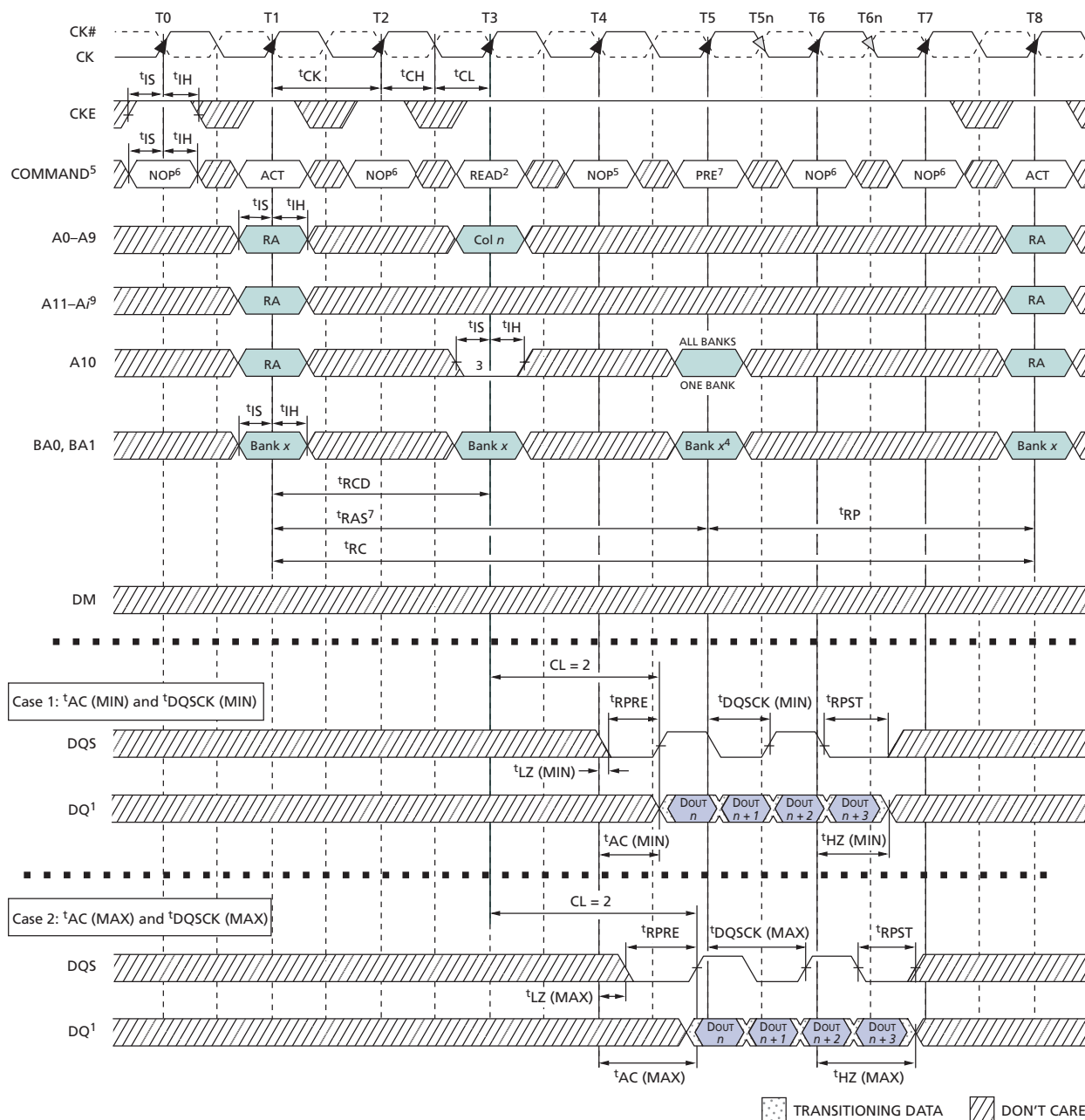
Notes: 1. DOUTn = data out from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T5 if ^{t}RAS minimum is met.
8. Refer to Figure 38 on page 66 and Figure 39 on page 67 for DQS and DQ timing details.
9. i = the most significant column address bit for each configuration.

Figure 47: Bank Read – with Auto Precharge
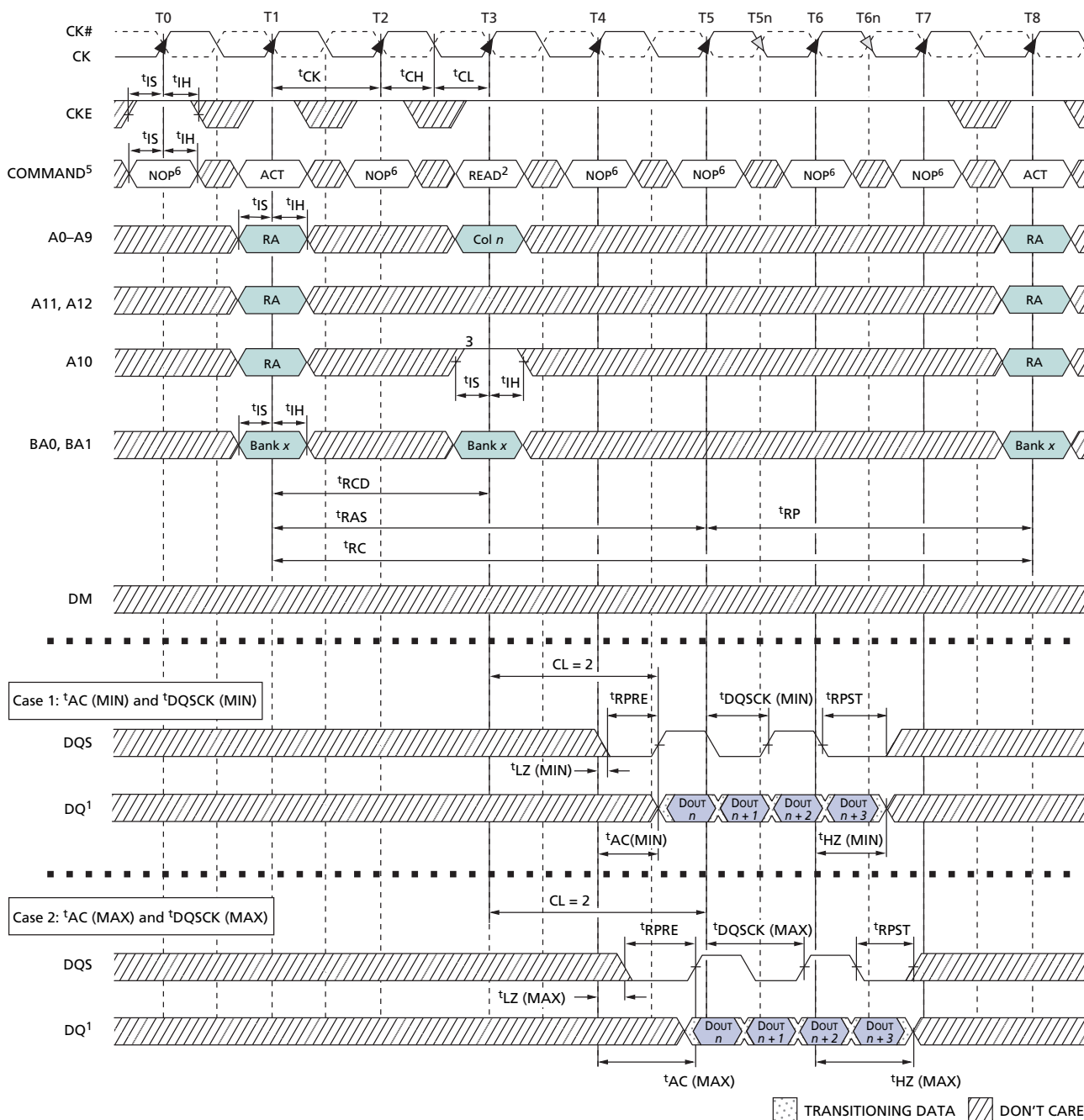
Notes:
1. D$_{OUT}$ n = data-out from column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. Refer to Figure 38 on page 66 and Figure 39 on page 67 for detailed DQS and DQ timing.

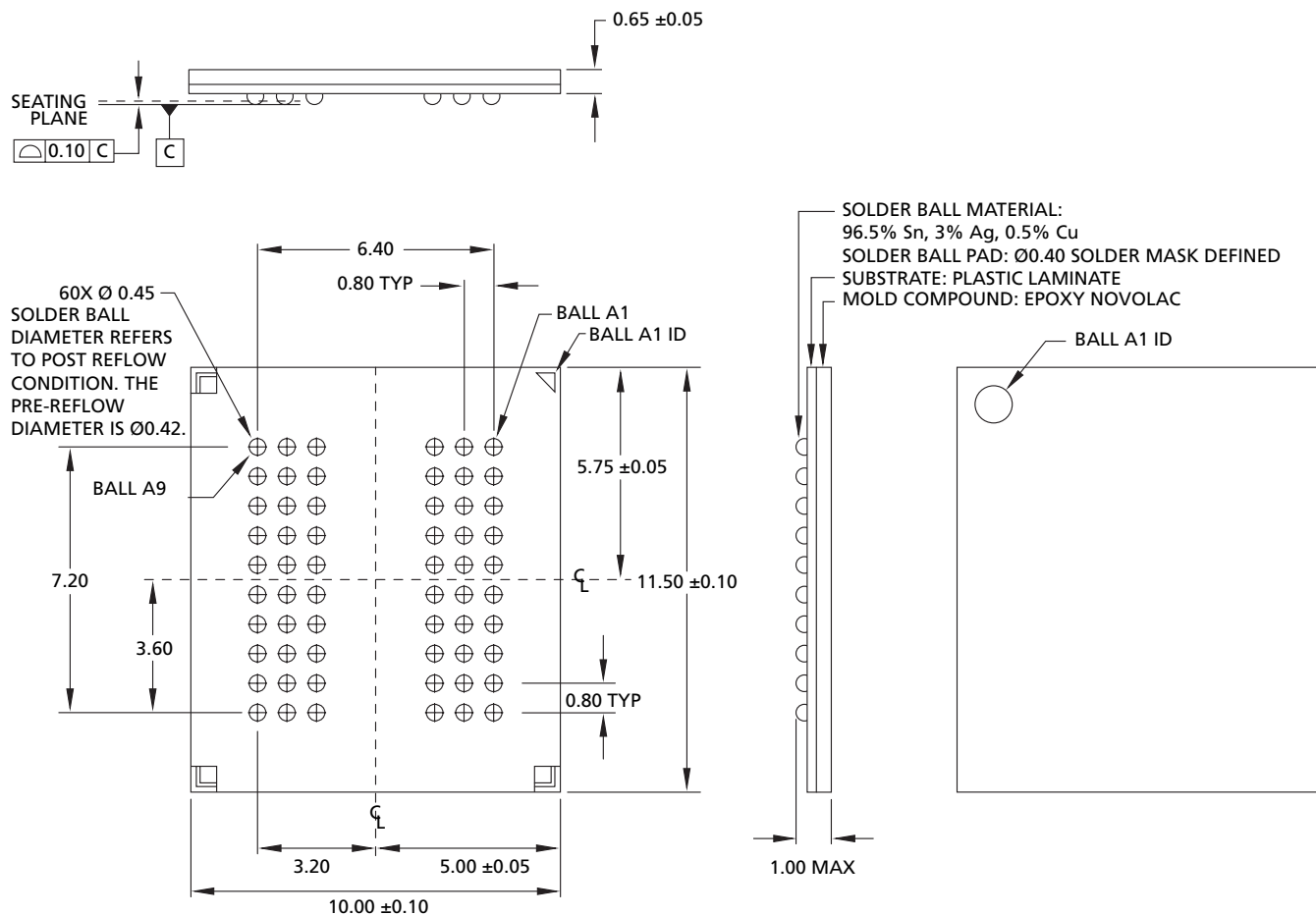**Figure 48:   Bank Write – Without Auto Precharge**
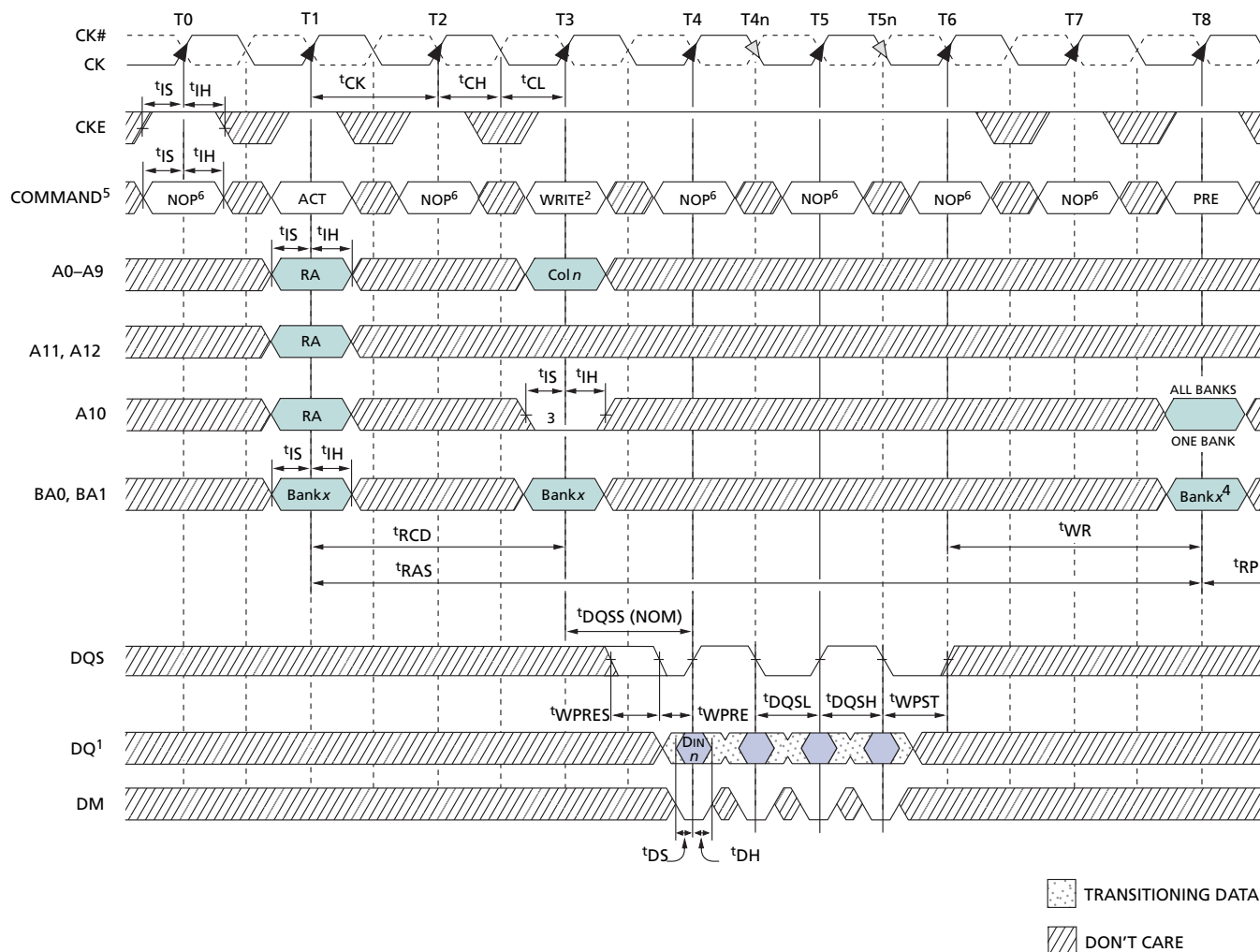
Notes: 1. D_{OUT} *n* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T4 or T5.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.

Figure 49: Bank Write – with Auto Precharge

Notes:
1. D_{OUT} n = data-out from column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T4 or T5.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.

Figure 50: Write – DM Operation
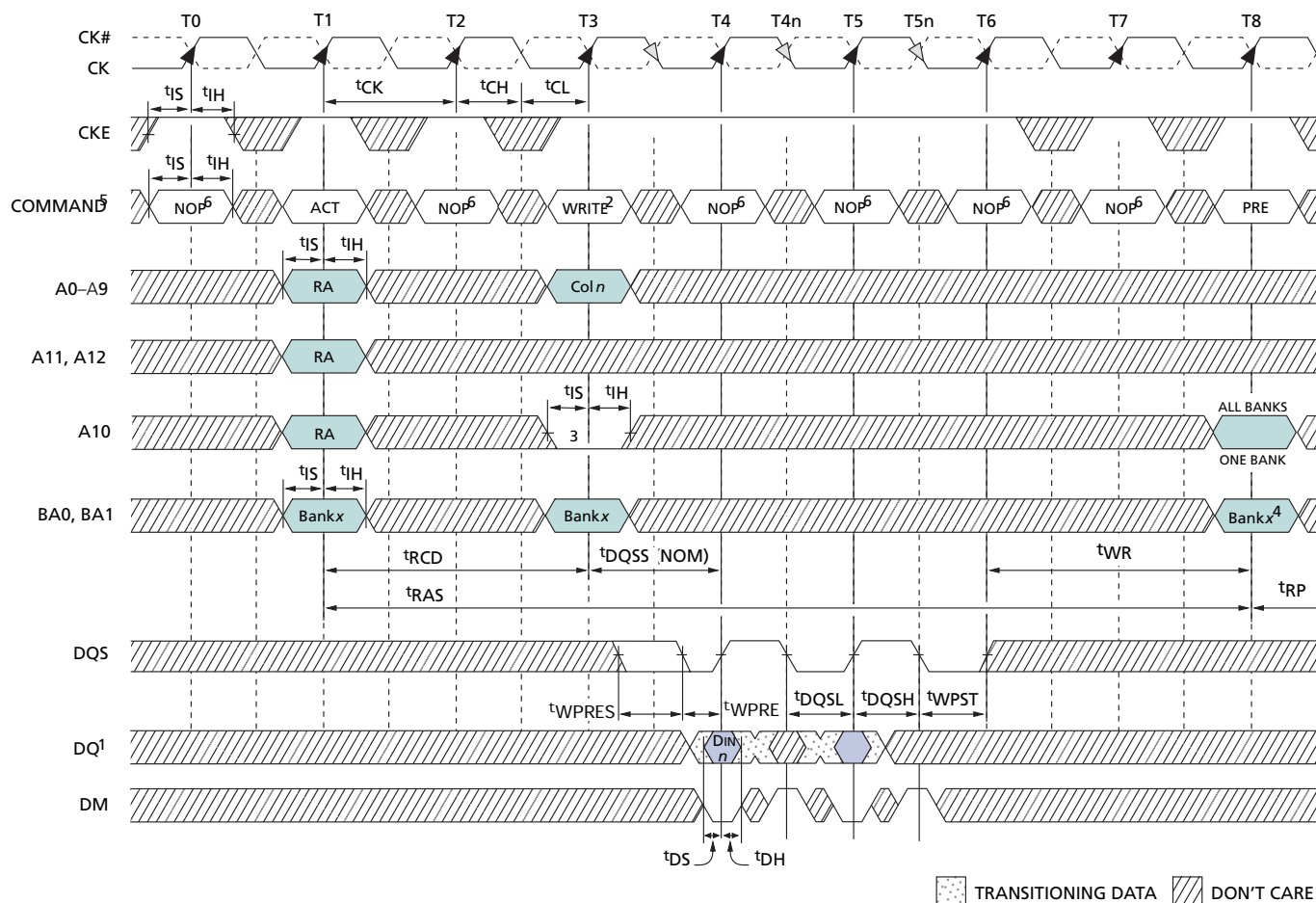
TRANSITIONING DATA   DON'T CARE

Notes:
1. D_{OUT} n = data-out from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^tDSH is applicable during ^tDQSS (MIN) and is referenced from CK T4 or T5.
8. ^tDSH is applicable during ^tDQSS (MIN) and is referenced from CK T5 or T6.

Package Dimensions

Figure 51:   60-Ball VFBGA Package

Notes: 1.   All dimensions are in millimeters.

Figure 52: 90-Ball VFBGA Package

Notes: 1. All dimensions are in millimeters.